	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L6	262	(219/634).CCLS.	USPAT	2003/08/11 19:09
2	IS&R	L7	0	(219/635).CCLS.	USPAT	2003/08/11 19:09
3	IS&R	L8	123	(219/647).CCLS.	USPAT	2003/08/11 19:10
4	IS&R	L10	153	(219/671).CCLS.	USPAT	2003/08/11 19:11
5	IS&R	L11	103	(219/675).CCLS.	USPAT	2003/08/11 19:10
6	IS&R	L12	94	(219/638).CCLS.	USPAT	2003/08/11 19:12
7	IS&R	L13	568	(118/723I,723IR).CCLS.	USPAT	2003/08/11 19:12
8	IS&R	L14	287	(156/345.48).CCLS.	USPAT	2003/08/11 19:12
9	IS&R	L15	606	(438/487,488).CCLS.	USPAT	2003/08/11 19:13
10	IS&R	L16	1002	(117/94,95,954).CCLS.	USPAT	2003/08/11 19:13
11	BRS	L17	2929	6 or 7 or 8 or 9 or 10 or 11 or 12 or 13 or 14 or 15 or 16	USPAT	2003/08/11 19:14
12	BRS	L18	57	((induction near coil$1) with semiconductor) and substrate$1	USPAT	2003/08/11 19:15
13	BRS	L19	123	((induction near coil$1) with semiconductor)	USPAT	2003/08/11 19:15
14	BRS	L20	11	19 and susceptor$1	USPAT	2003/08/11 19:16
15	BRS	L21	2	20 and ((glass or plastic or quartz) with substrate$1)	USPAT	2003/08/11 19:17
16	BRS	L22	4	20 and ((glass or plastic or quartz) with susceptor$1)	USPAT	2003/08/11 19:17

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United States Patent [19]

Sasaki et al.

[11] Patent Number: 5,970,368

[45] Date of Patent: Oct. 19, 1999

[54] **METHOD FOR MANUFACTURING POLYCRYSTAL SEMICONDUCTOR FILM**

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[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

[21] Appl. No.: **08/939,660**

[22] Filed: **Sep. 29, 1997**

[30] **Foreign Application Priority Data**

Sep. 30, 1996 [JP] Japan 8-259529
Mar. 14, 1997 [JP] Japan 9-061072

[51] **Int. Cl.**[6] **H01L 21/205**; H01L 29/04

[52] **U.S. Cl.** ..... **438/487**; 438/488; 156/617 R; 156/620

[58] **Field of Search** ..... 438/488, 150, 438/487; 156/617 R, 620

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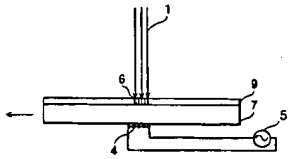
Primary Examiner—Charles Bowers
Assistant Examiner—Martin Sulsky
Attorney, Agent, or Firm—Oblon, Spivak McClelland, Maier & Neustadt, P.C.

[57] **ABSTRACT**

There is disclosed a method for manufacturing a polycrystal semiconductor film comprising the steps of applying a high energy beam to a surface of a semiconductor film comprising an amorphous or a polycrystal semiconductor provided on a surface of a substrate to melt only the semiconductor film, and solidifying the film via a solid and liquid coexisting state to form a semiconductor film comprising a polycrystal semiconductor having a large grain diameter, by heating a liquid part using a difference in an electric resistance in the liquid and solid coexisting state to heat only the liquid part, and by extending the solidification time until the completion of solidifying of the molten liquid crystal film. Furthermore, as the base film of the semiconductor film, a material having a melting point of 1600° C. and a thermal conductivity of 0.01 cal/cm.s.° C. is used to suppress heat dissipation from the molten liquid of the semiconductor to the substrate so that time until the complete solidification can be prolonged. Furthermore, the beam is irradiated so as to form a standing wave at a predetermined position of the surface of the semiconductor film to generate the heat density distribution having the same cycle with the standing wave and to melt the semiconductor film with the result that a polycrystal semiconductor film comprising a uniform and a large crystal grains by controlling the distribution of the crystal nuclei at the interface between the base film and the substrate.

18 Claims, 17 Drawing Sheets



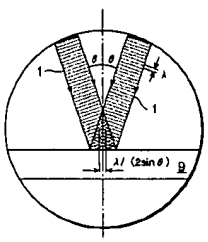


FIG.1A

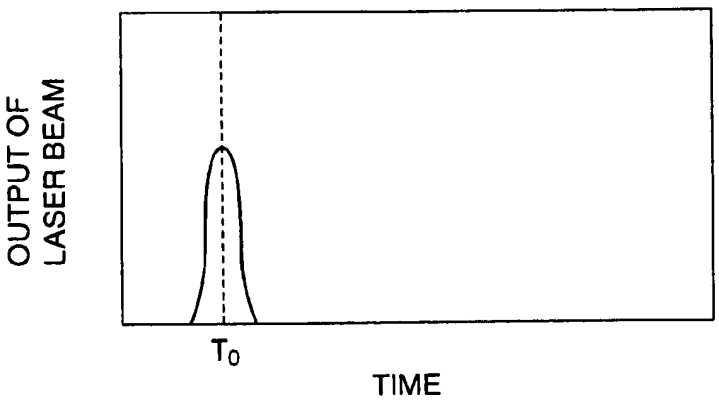


FIG.1B

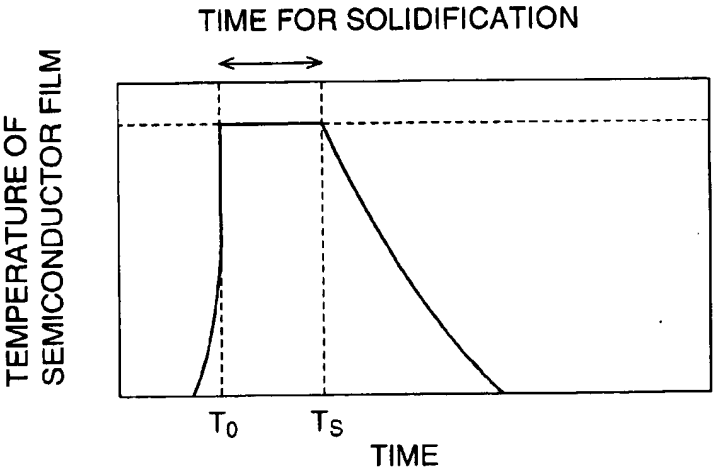
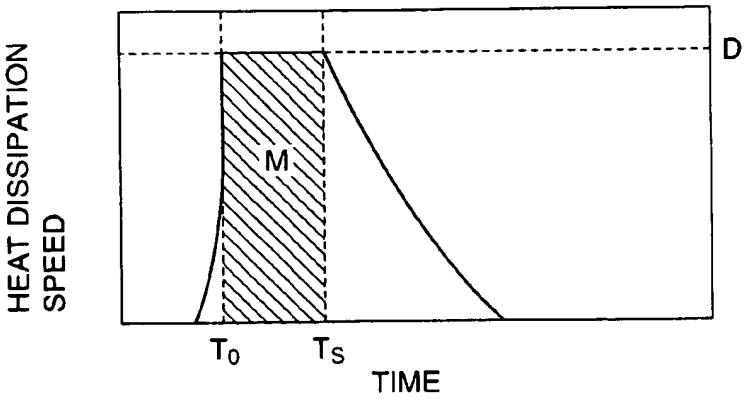


FIG.1C



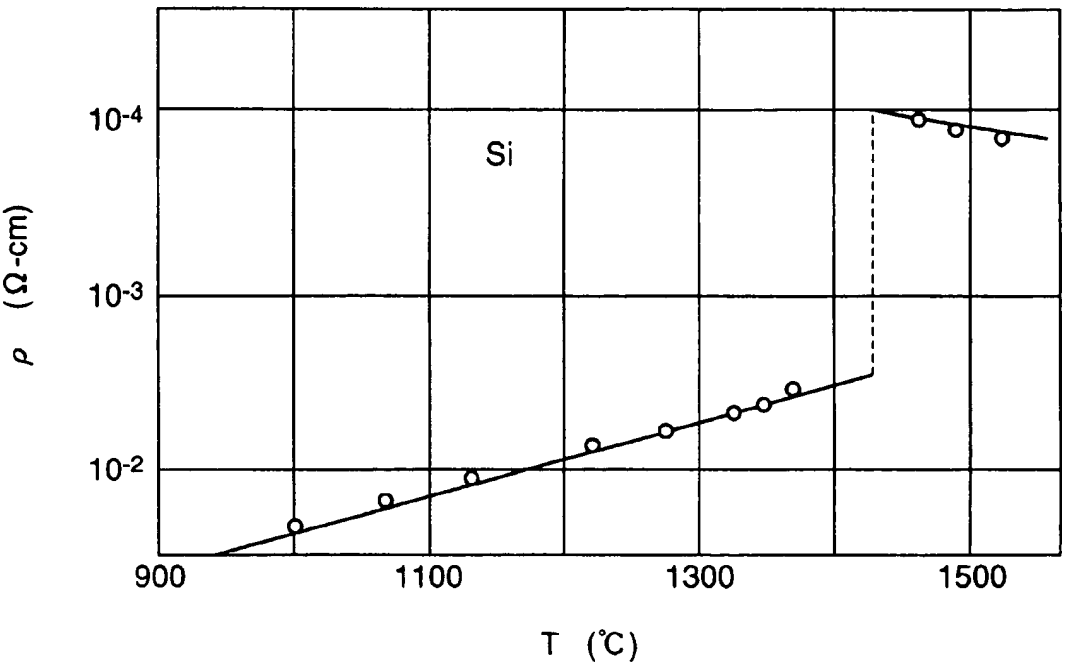


FIG.2

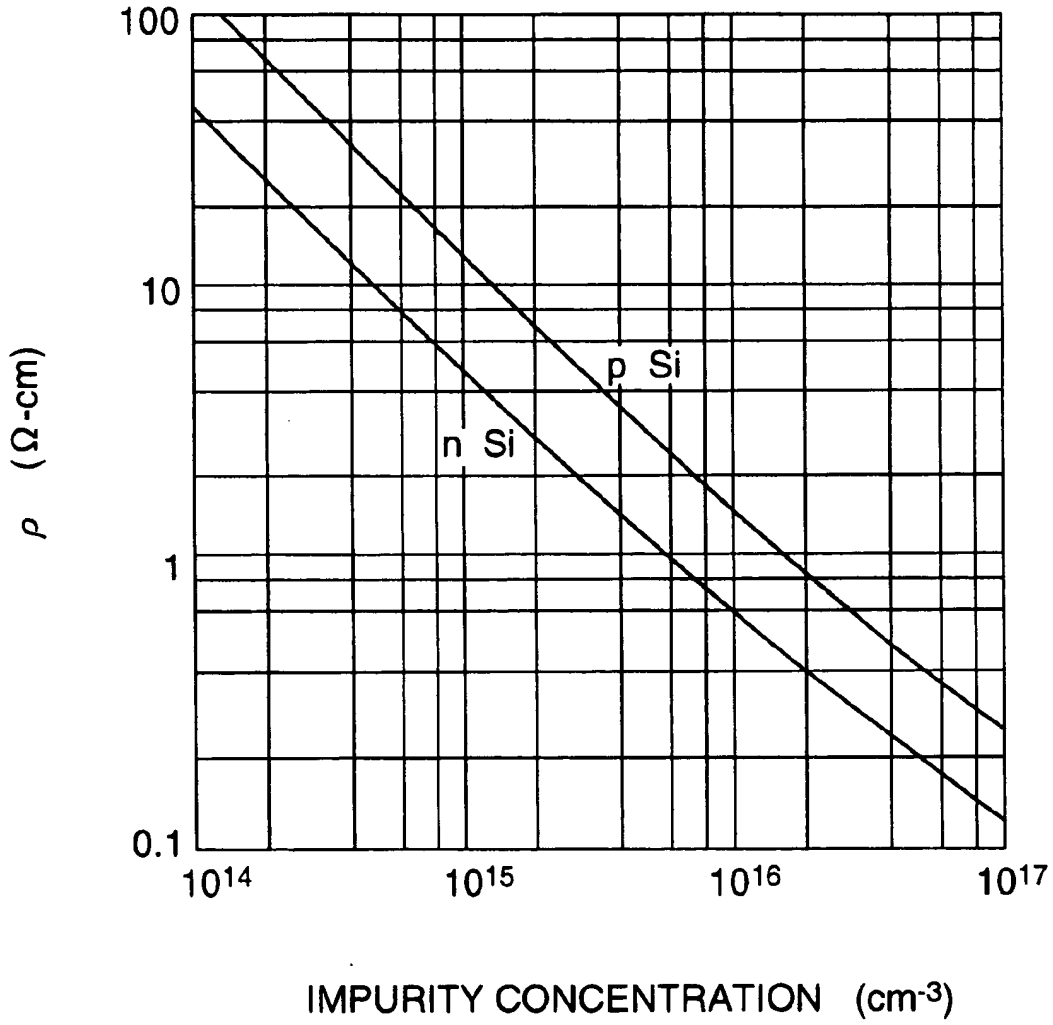

100
10
1
0.1
ρ (Ω-cm)
p Si
n Si
10^14
10^15
10^16
10^17
IMPURITY CONCENTRATION (cm^-3)

FIG.3

FIG.4A

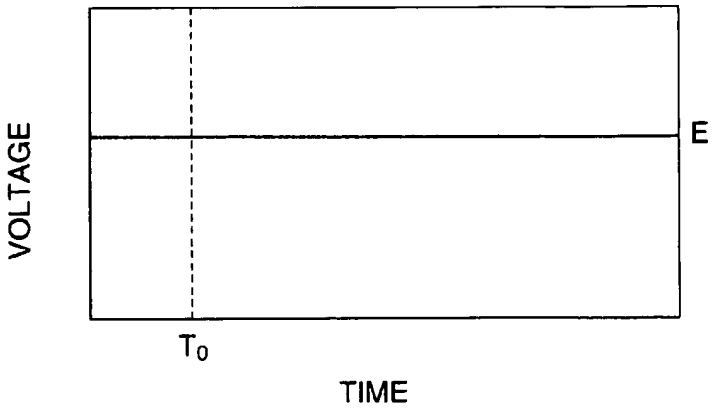


FIG.4B

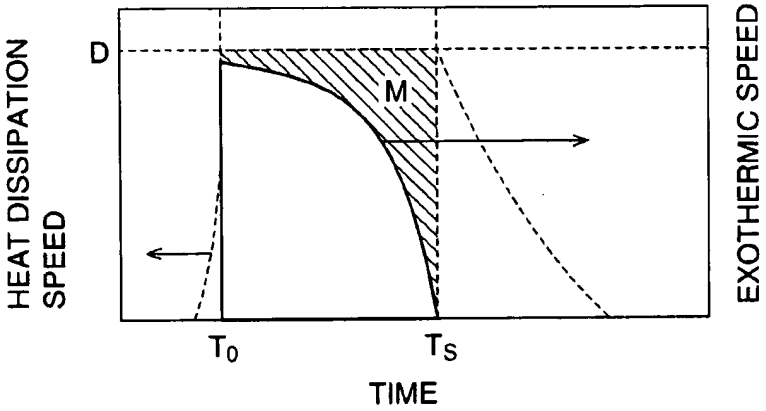
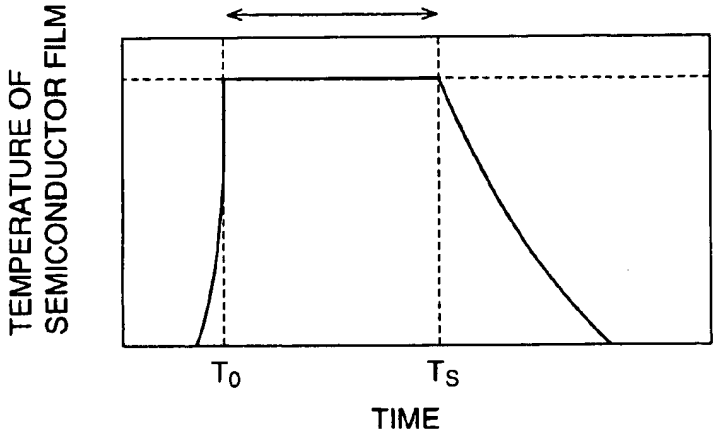


FIG.4C



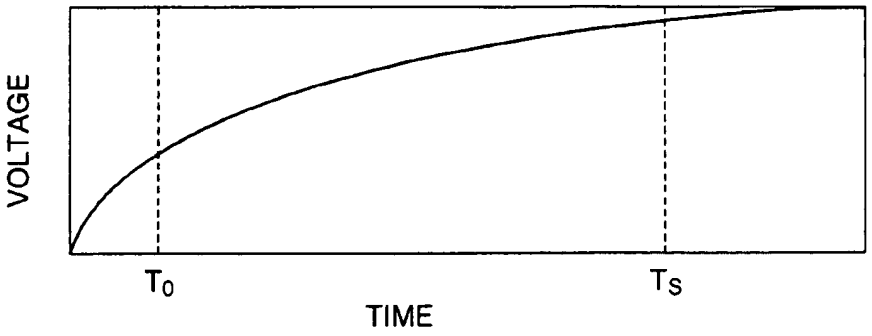


FIG.5A

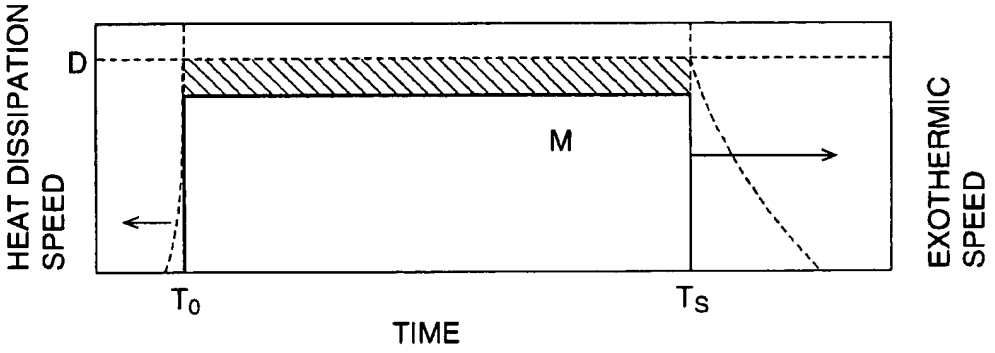


FIG.5B

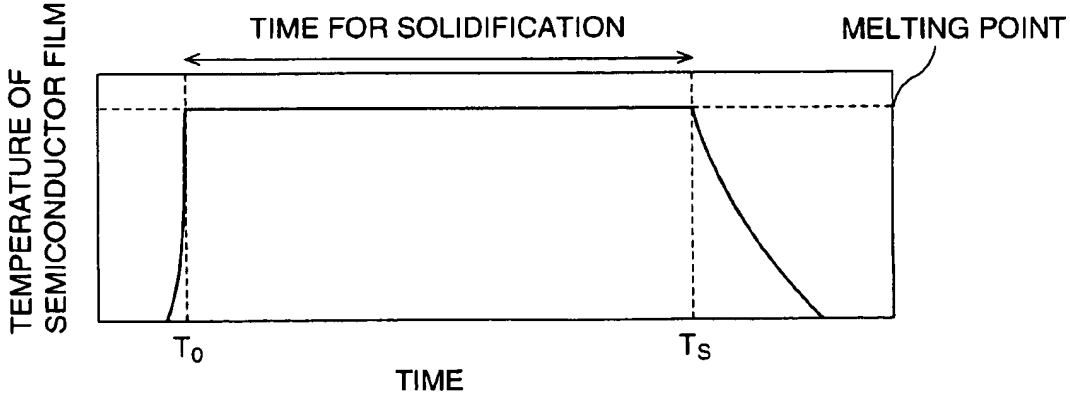


FIG.5C

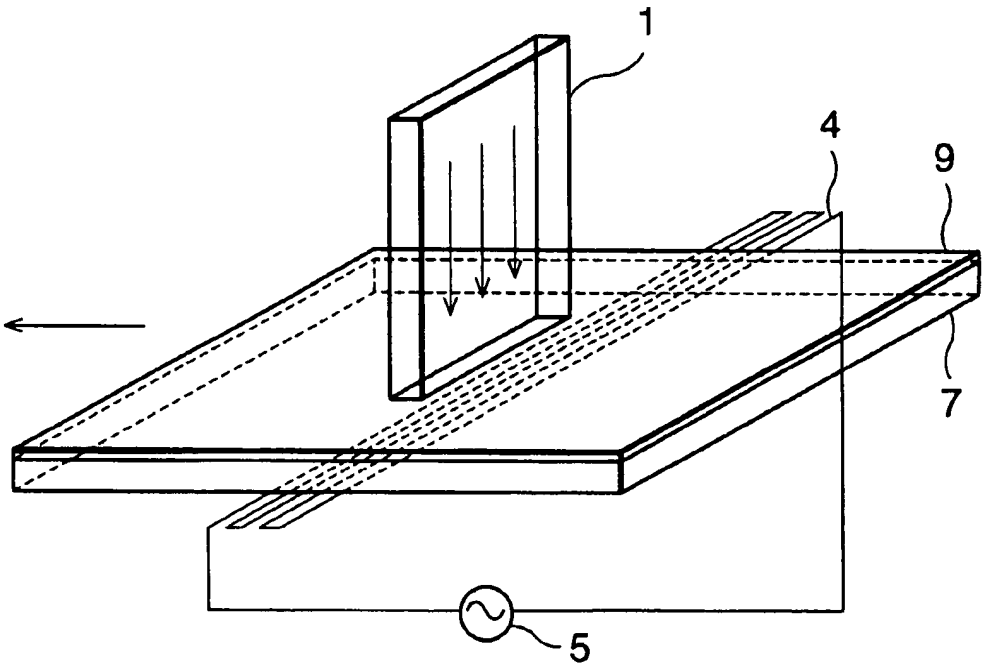


FIG.6A

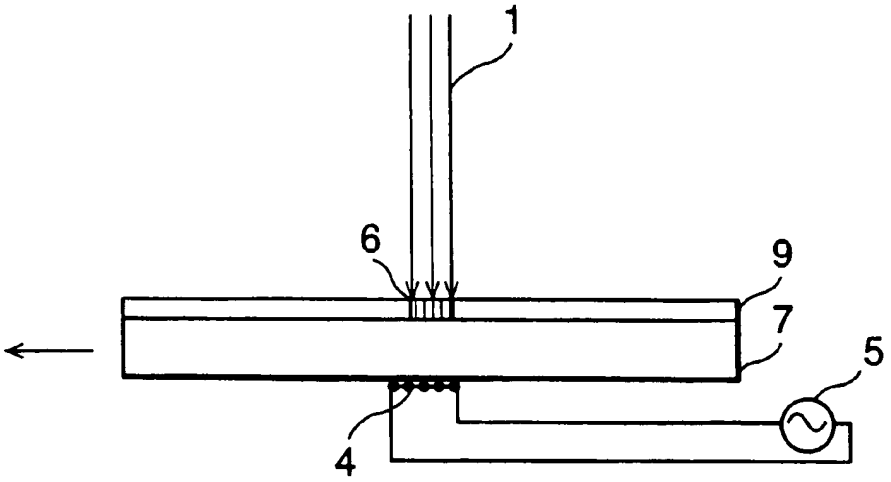


FIG.6B

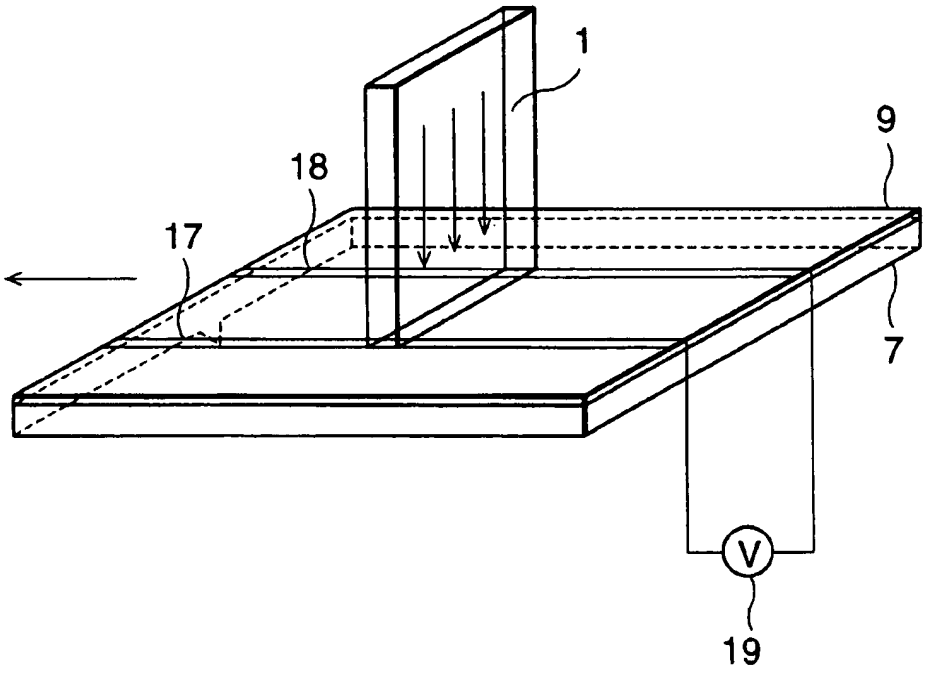


FIG.7A

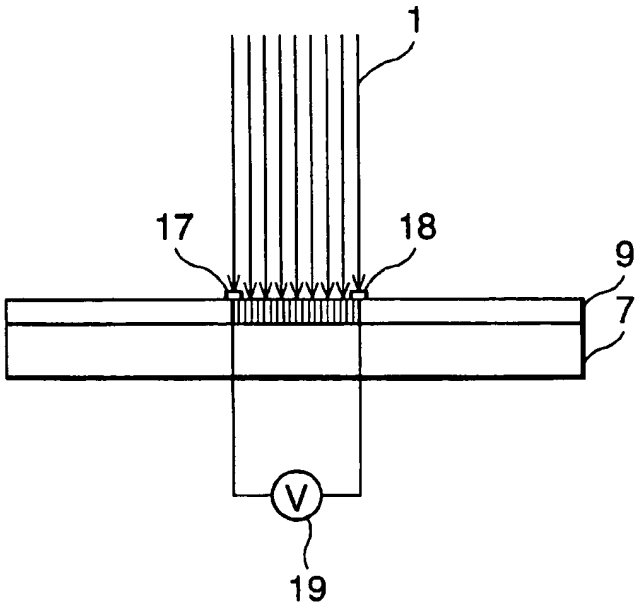


FIG.7B

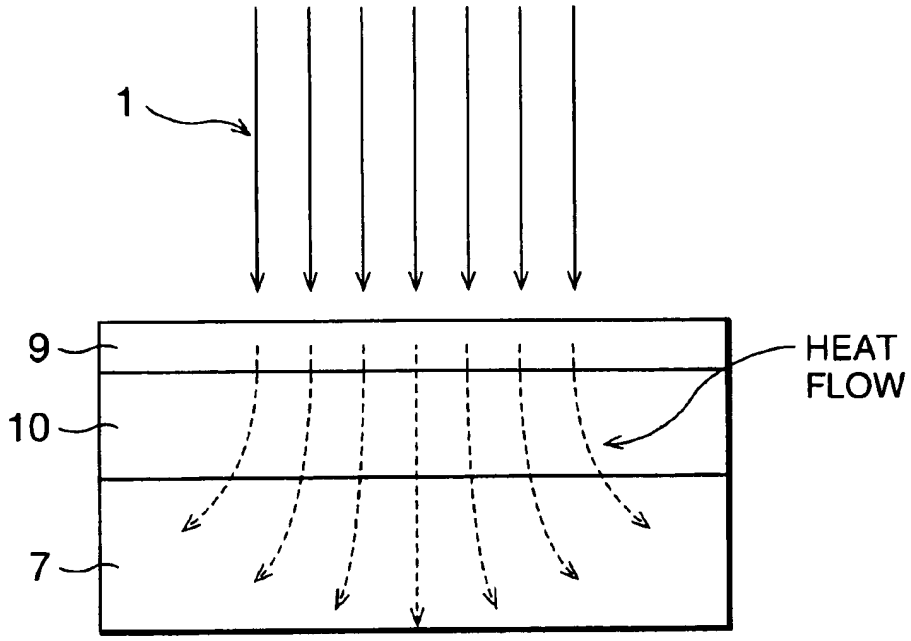


FIG.8

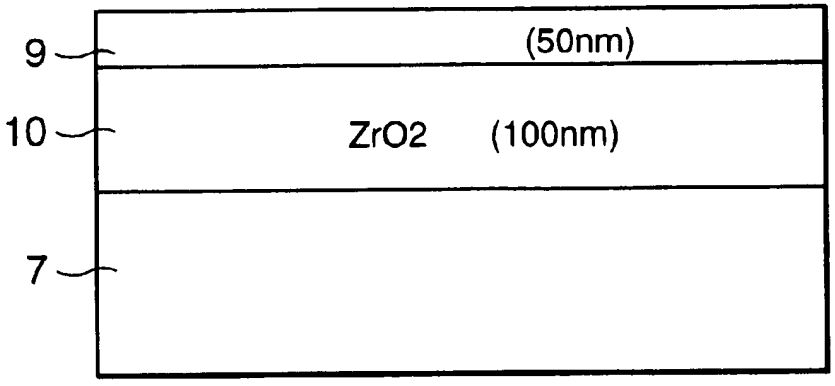


FIG.9

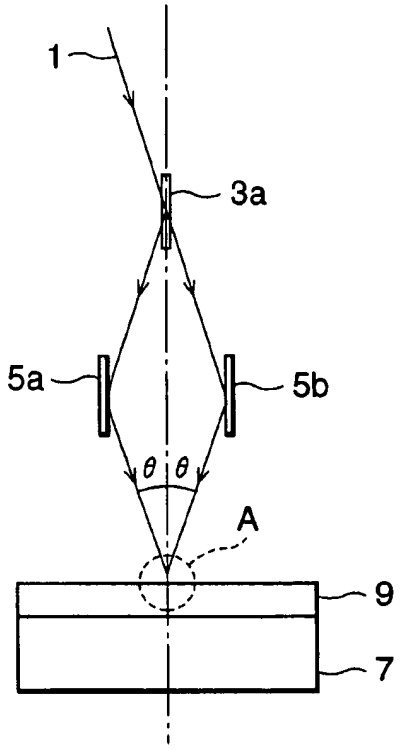


FIG.10A

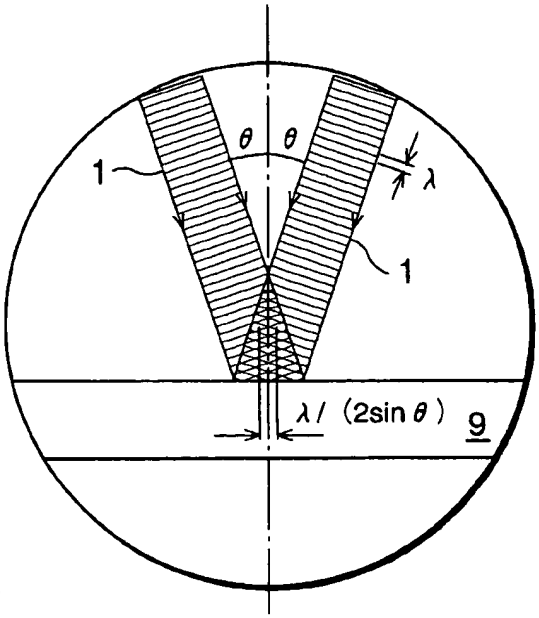


FIG.10B

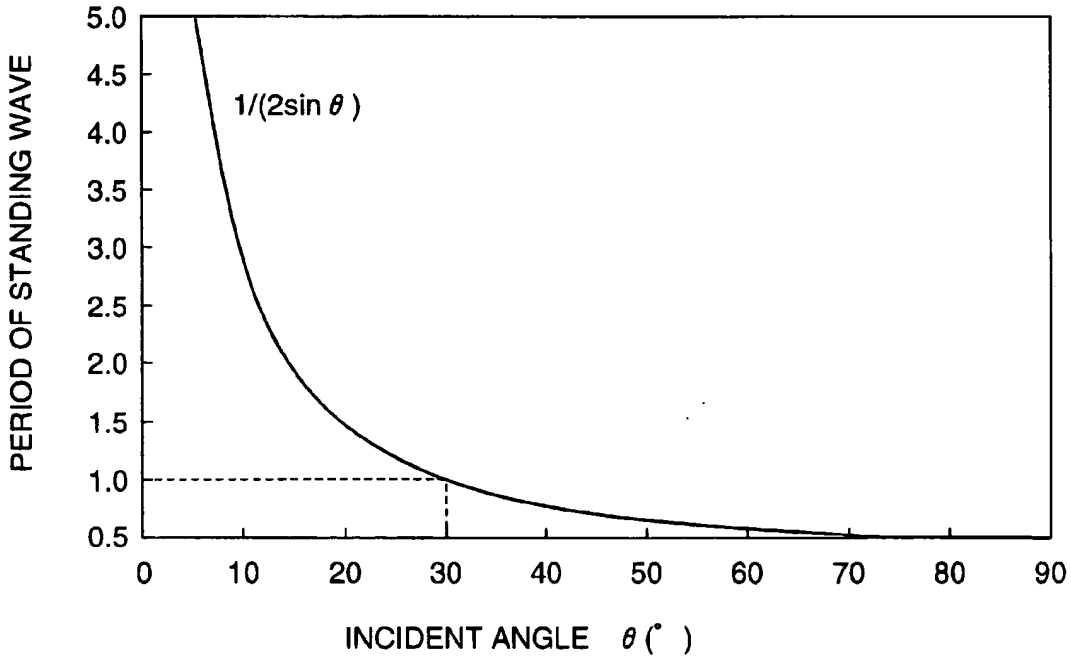

PERIOD OF STANDING WAVE
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
1/(2sin θ)
0
10
20
30
40
50
60
70
80
90
INCIDENT ANGLE θ (°)

FIG.11

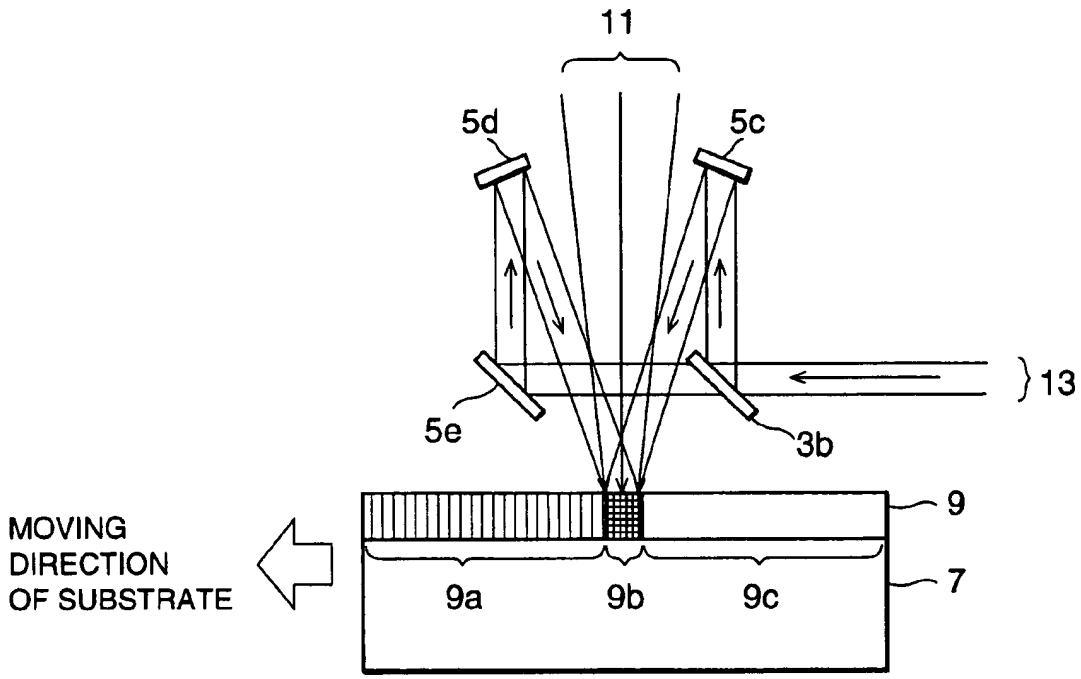


FIG.12

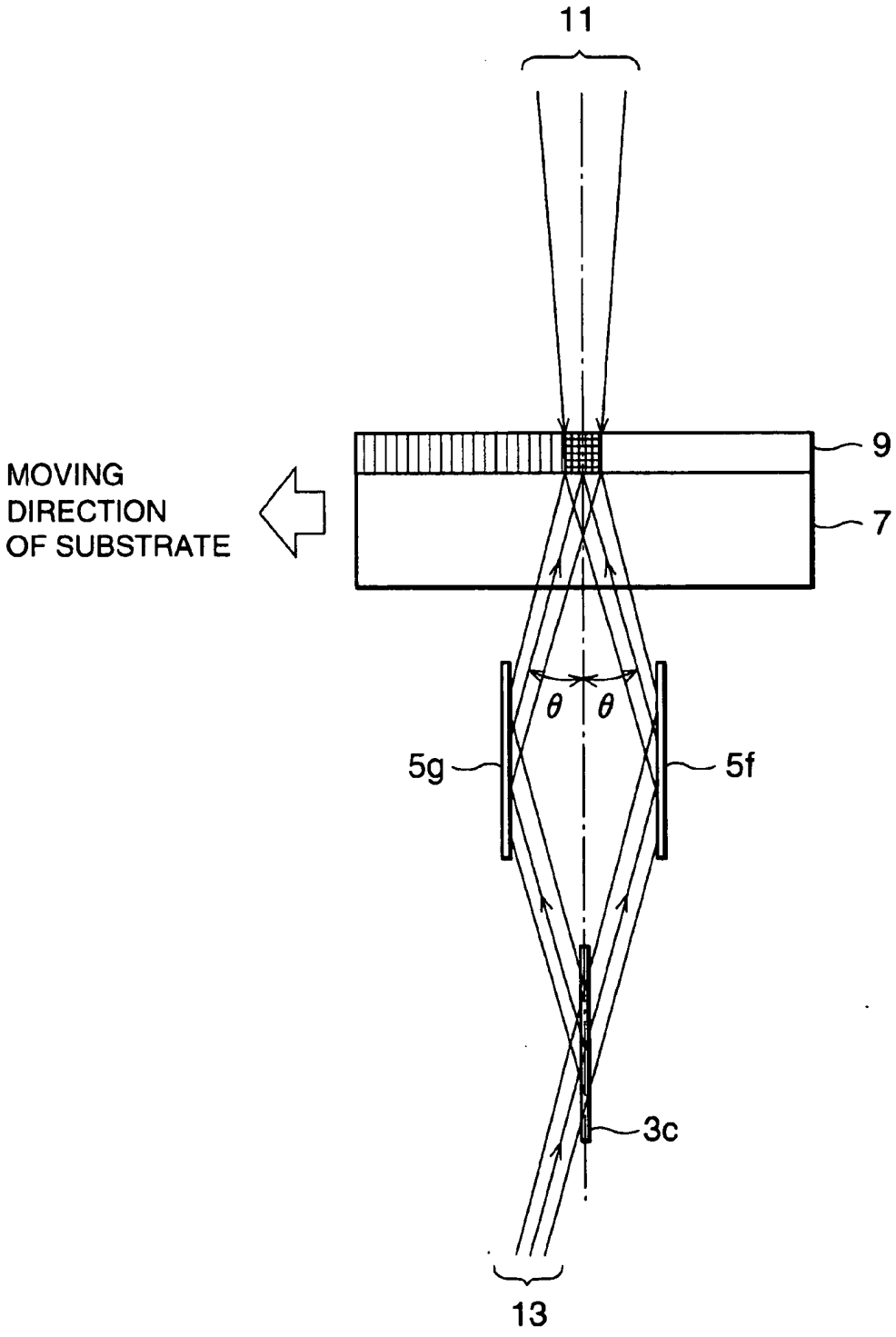


FIG.13

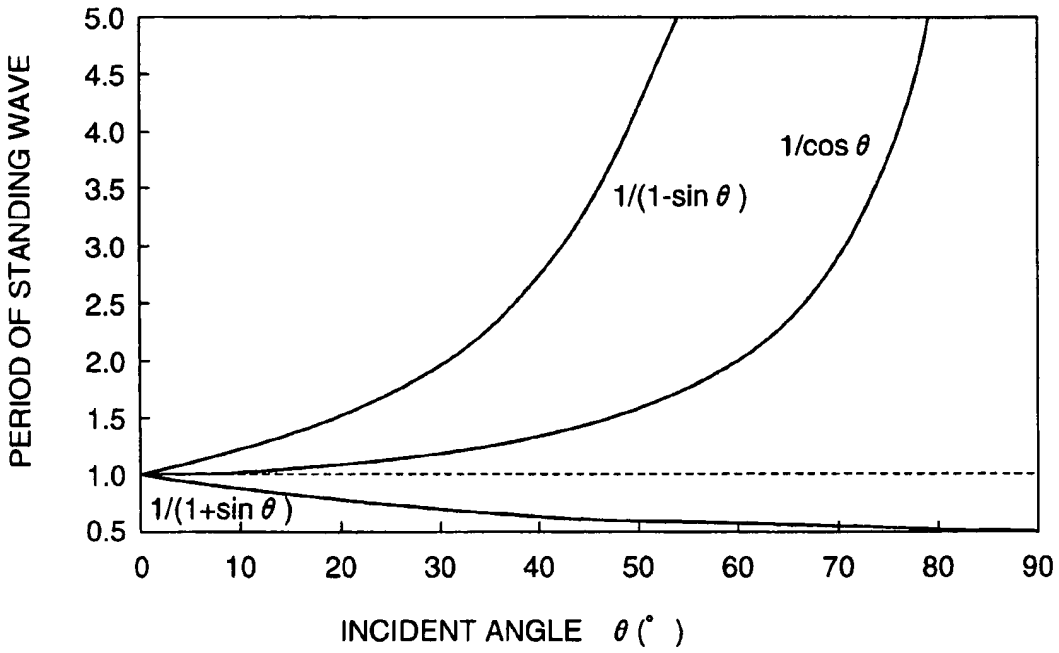

PERIOD OF STANDING WAVE
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
10
20
30
40
50
60
70
80
90
1/cos θ
1/(1-sin θ)
1/(1+sin θ)
INCIDENT ANGLE θ (°)

FIG.14

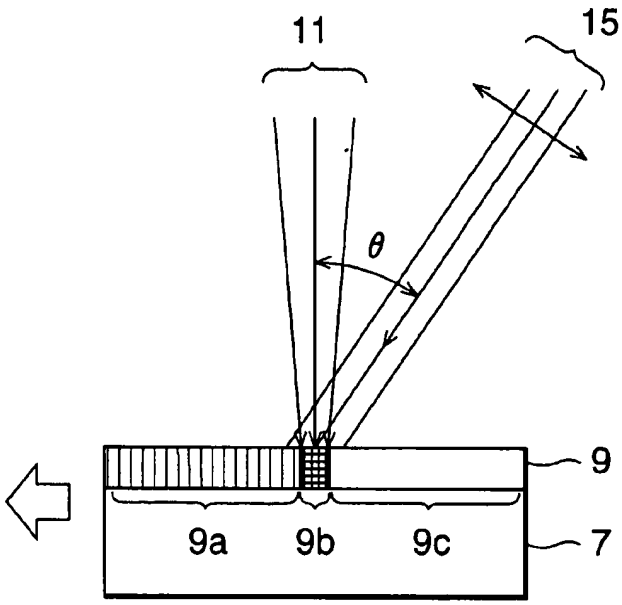


FIG.15A

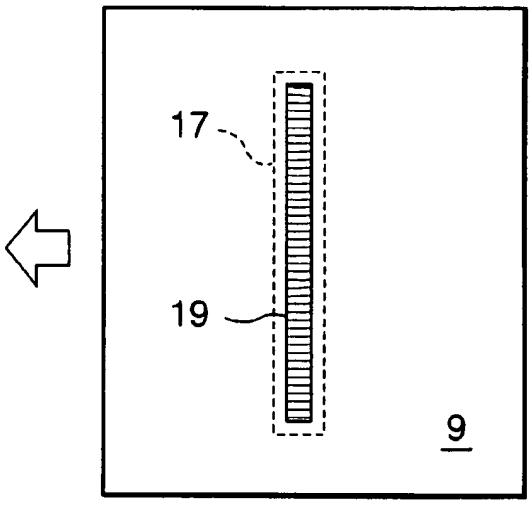


FIG.15B

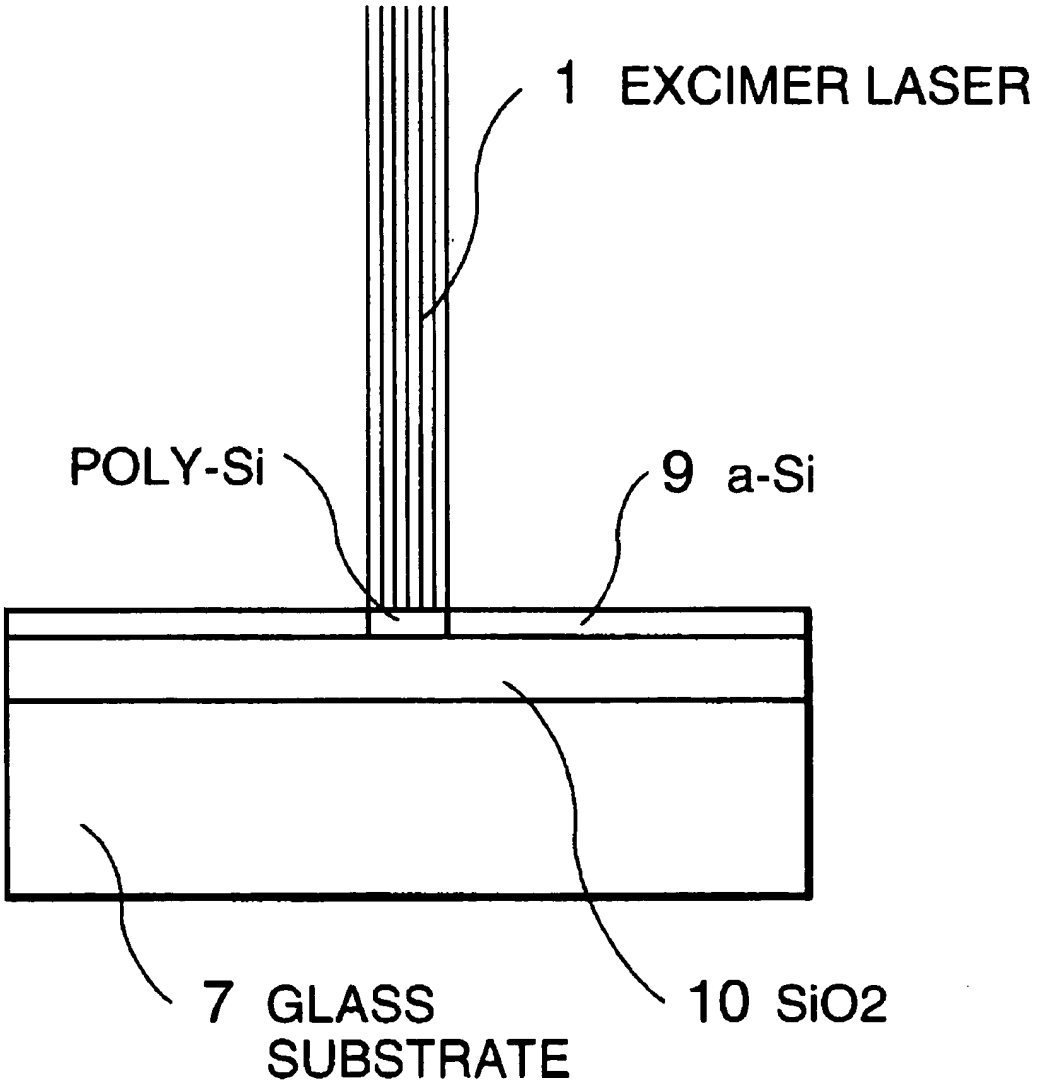


FIG.16
PRIOR ART

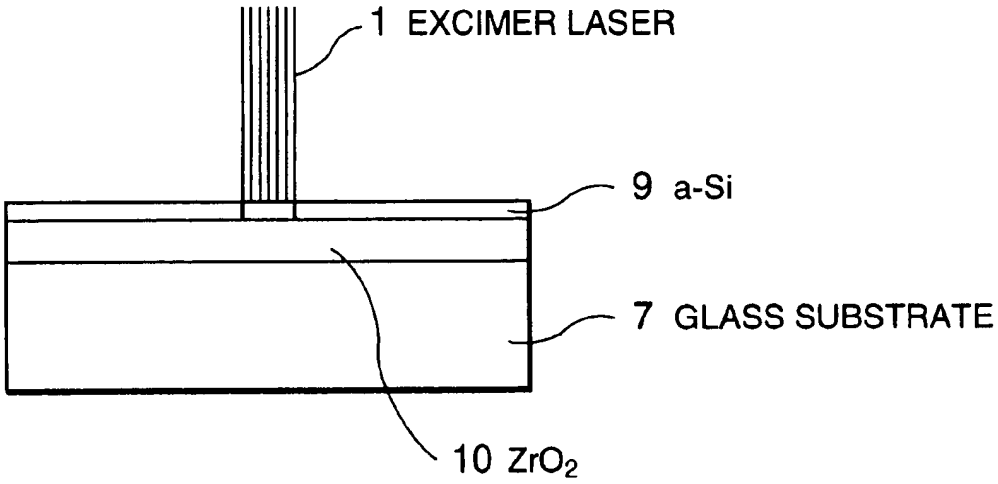

1 EXCIMER LASER
9 a-Si
7 GLASS SUBSTRATE
10 ZrO_2

FIG.17

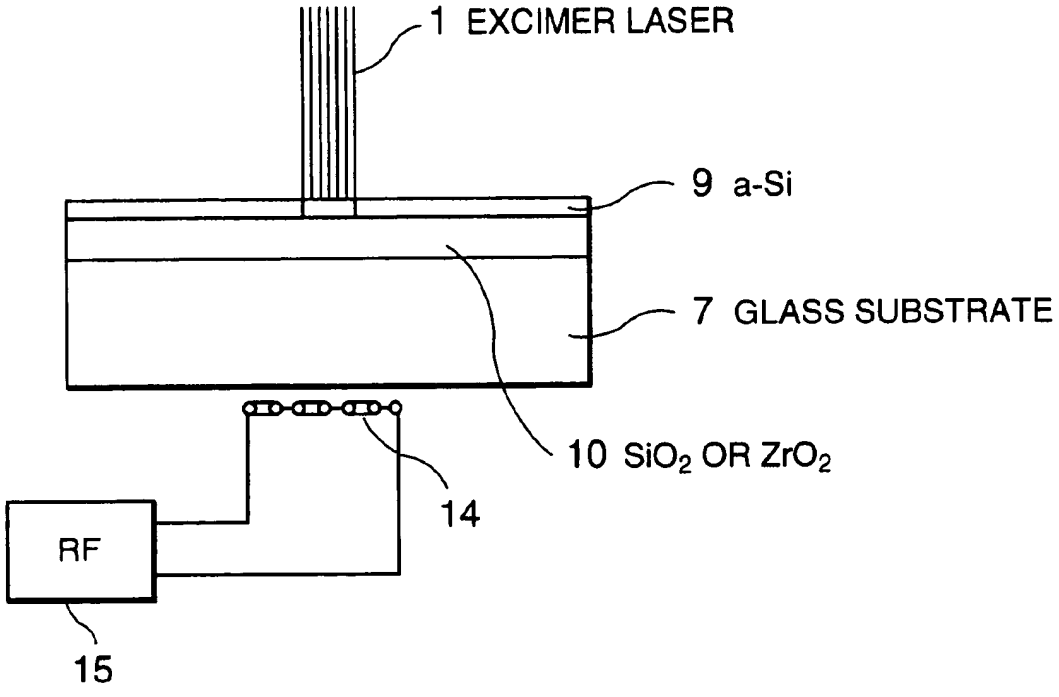

1 EXCIMER LASER
9 a-Si
7 GLASS SUBSTRATE
10 SiO_2 OR ZrO_2
14
RF
15

FIG.18

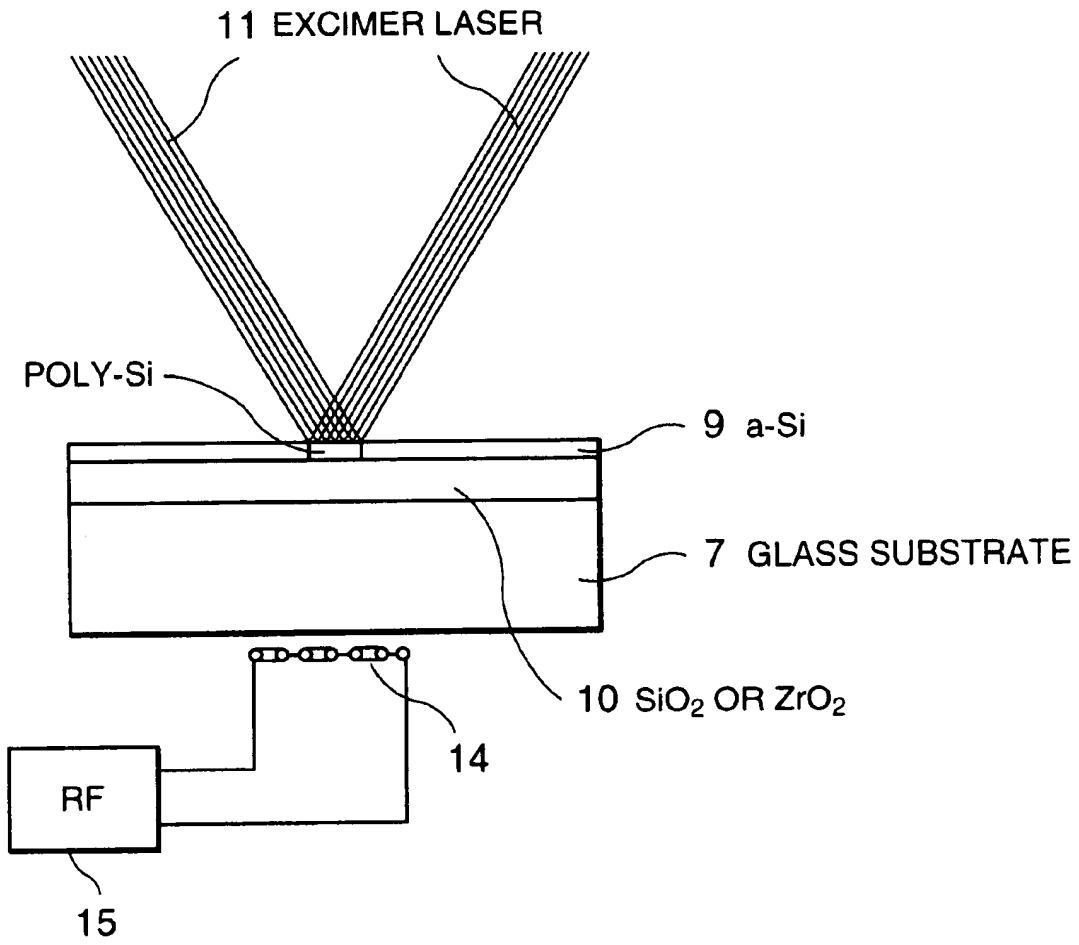

11 EXCIMER LASER
POLY-Si
9 a-Si
7 GLASS SUBSTRATE
10 SiO_2 OR ZrO_2
14
RF
15

FIG.19

METHOD FOR MANUFACTURING POLYCRYSTAL SEMICONDUCTOR FILM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing a polycrysal semiconductor film used in a liquid crystal display device and the like, and more particularly to a method for manufacturing a polycrystal semiconductor film having crystal grains with a large and even diameter.

2. Description of the Related Art

Thin film transistors (hereinafter referred to as TFT) are normally formed on a polycrystal semiconductor film formed on a substrate such as a quarz substrate, a glass substrate or the like.

Semiconductor characteristics such as mobility of the polycrystal semiconductor film and the like are improved with an increase in the size of crystal grains. Consequently, in the case that a quarz glass having an excellent heat-resistance property is used as a substrate, and in the case that the damage of the substrate does not hinder the usage thereof, for example, such as a solar battery, there is used a method in which the substrate of an amorphous Si-film (hereinafter referred to as a-Si film) is heated as it is so that the semiconductor film is molten followed by holding the film in a heated state for a long time to anneal and to carry out a polycrystallization.

However, when the film is used as a TFT device of the liquid crystal display device, the quarz is very expensive with the result that the cost of the TFT becomes high. Consequently, the TFT device is consequently formed on the cheap glass substrate.

Here, when a polycrystal Si is used for the TFT device of the liquid crystal display device, a long-time high temperature annealing is required (for example heating for 8 to 56 hours in the atmosphere of a high temperature nitrogen at 600° C. or more). However, in the case of the glass substrate, a deformation or a warp is generated.

Consequently, there is normally used a pulse laser irradiation method in which only the semiconductor film is heated and molten in a short time by applying an excimer pulse laser to the amorphous semiconductor film or the semiconductor film comprising a fine crystal polycrystal on the glass substrate with the result that a polycrystal film with a large grain size.

In other words, in the polycrystallization using an excimer laser, more than several 10 nanosecond pulses are irradiated to a surface of the semiconductor film such as the a-Si (amorphous Si) film which is deposited on the surface of the substrate to melt only the film and provide a solid state via a mixed state of a solid phase and a liquid phase thereby forming a polycrystal film.

However, as described above, the excimer laser annealing can melt only the semiconductor film such as the a-Si film or the polycrystal Si film by applying more than several 10 nano second laser pulse to the film surface. However, there arises a problem in that the heat dissipation to the substrate is very fast so that time up to the completion of solidification is short and the crystal grain cannot be grown to a large size. It is necessary to take as long time as possible up to the solidification to grow the crystal grains to an even and large diameter.

However, it is possible to prolong the time required for the solidification by prolonging the pulse length of the laser, and prolonging the heat input time with a multiple pulse using a plurality of lasers. For all that, a single pulse length can be prolonged only by several times, so that the time up to the completion of the solidification cannot be prolonged on a large scale. Furthermore, a multiple pulse method using a plurality of lasers is an effective method in principle, but controlling a plurality of unstable lasers at the same time was virtually impossible.

Furthermore, in a simple method, the solidification time can be prolonged to some extent by applying a laser in a state in which the substrate is heated to an extent which does not affect the glass (300 to 500° C.). However, in the method, a large effect cannot be provided unless the substrate is heated to a temperature approximate to the melting point of the semiconductor. It was impossible to prolong the solidification time to a large extent up at a temperature of 300 to 500° C. which is a heat resistant temperature in the usage of the glass substrate.

In this manner, the formation of the polycrystal semiconductor film using the conventional pulse laser has a problem in that the solidification time is extremely short until the end of the solidification and the crystal grains cannot be grown to a large size.

Another problem is that when the film is completely molten to the substrate or to the interface with the base film at the time of melting the semiconductor film such as a-Si film or the polycrystal Si film or the like with the excimer laser, crystal nuclei at the interface which constitute seeds of crystallization have disappeared and the molten liquid is supercooled at the time of cooling with the result that a large number of crystal nuclei are abruptly generated from the interface and from within the molten liquid and crystal grains with a large grain size are not generated, a polycrystal semiconductor film comprising a plurality of fine crystals is provided and semiconductor properties such as required mobility or the like are not obtained.

On the contrary when the melting of the semiconductor film is insufficient, a large number of crystal nuclei remain at an interface with the substrate or the base film so that a crystal growth proceeds with the residual crystal nuclei as seeds and fine crystal grains, which have a grain diameter d which is in an inverse proportion to the density (N) of the residual nuclei, are generated.

When a relation between the intensity of the laser beam and the residual nuclei is described, the density of the residual nuclei decreases with an increase in the intensity of the laser beam so that the size of the crystal increases until the intensity of the laser beam increases, the semiconductor film is completely molten and the residual nuclei completely disappear.

However, when the intensity of the laser beam attains a maximum limit, the residual nuclei disappear, and, the supercooling is generated in the process of cooling with the result that fine crystallization is generated.

Therefore, in order to generate large crystal grains in a uniform manner, the control of the density of the residual nuclei and the generation position of the nuclei are important. However, in the method for manufacturing the polycrystal semiconductor film by means of the conventional excimer laser annealing, a size of crystal grains which are generated largely change with a fine variation of the intensity of the laser beam in the vicinity of a maximum value so that the polycrystal semiconductor having a stable and uniform large crystal grains could not be supplied.

SUMMARY OF THE INVENTION

The present invention has been made to solve the aforementioned problems.

A first object of the invention is to provide a method for forming a polycrystal semiconductor film in which the solidification is completed from the molten state after the laser irradiation and the solidification time can be prolonged until polycrystallization so that a polycrystal semiconductor film is formed, which has even and large crystal grains in the manufacture of the polycrystal semiconductor film by pulse laser annealing.

A second object of the invention is to provide a method for manufacturing a polycrystal semiconductor film comprising even and large crystal grains having a size of several μm order by realizing a light intensity distribution with a period of several μm on the surface of the amorphous or a polycrystal semiconductor film in the manufacture of the polycrystal semiconductor film by the pulse laser to control the residual nuclei at the interface between the base film and the amorphous or polycrystal semiconductor film in a period of several μm.

The method for manufacturing the polycrystal semiconductor film according to a first aspect of the invention comprises the steps of irradiating a high energy pulse beam onto a surface of a semiconductor film comprising an amorphous or first polycrystal semiconductor formed on a substrate to melt only the semiconductor film, and solidifying and forming the semiconductor film comprising polycrystal with large crystal grains via a solid-liquid coexisting state, wherein only a liquid part generated by the melting of the semiconductor film is heated by using a difference in an electric resistance between a solid part and a liquid part in the solid-liquid coexisting state so as to prolong the solidification time can be prolonged until the completion of the solidification of the semiconductor film.

Furthermore, the method for manufacturing the polycrystal semiconductor film according to the first aspect of the invention is characterized in that the liquid part of the semiconductor film is heated by electromagnetic induction heating method or electric heating method.

Furthermore, the aforementioned electromagnetic induction heating method is characterized in that a high frequency current is supplied to an induction heating coil provided on the rear surface of the substrate so that an alternate current magnetic field is generated in the semiconductor film with electromagnetic induction.

An area of the alternate current magnetic field generated by the electromagnetic induction is wider than the high energy pulse beam irradiating area so that only the molten, liquified and low resistant part are heated with electromagnetic induction.

Furthermore, the heat generation speed by electromagnetic induction heating is lower than the heat dissipation speed to the substrate from the molten semiconductor film.

Furthermore, the method is characterized in that an electric field or a frequency is controlled for heating the semiconductor film with electromagnetic induction in synchronization with the high energy pulse beam irradiation, heating of the aforementioned electromagnetic induction heating is corrected in correspondence to increase of resistance of the semiconductor film by the change of the ratio of the solid and the liquid along the progress of the solidification, and a constant heating state is held.

In another method for manufacturing the polycrystal semiconductor film according to the first aspect of the invention, a voltage is applied to a conductor provided adjacent to the aforementioned semiconductor film and the molten low resistant liquid part is heated.

Furthermore, the above method for manufacturing the aforementioned polycrystal semiconductor film is characterized in that only the semiconductor film part is electrified and heated wherein the aforementioned electrified area for heating and the aforementioned high energy beam application area overlap.

Furthermore, the aforementioned method for manufacturing the polycrystal semiconductor film is characterized in that a voltage is controlled for electrifying and heating the semiconductor film in synchronization with a high energy beam which is irradiated to a surface of the amorphous or polycrystal semiconductor film, and a lowering of the heating efficiency due to the increase of resistance which is generated by the change of the ratio of the solid and the liquid along the progress of the solidification is corrected to provide a constant heating state.

The method for manufacturing the polycrystal semiconductor film according to the second aspect of the present invention comprises irradiating a high energy beam onto a surface of an amorphous or a first polycrystal semiconductor film to melt the aforementioned semiconductor film, and further solidifying the semiconductor film to form a polycrystal film, wherein a material having a melting point of 1600° C. or more and having a heat conduction rate of 0.01 cal/cm.s.° C. is used as a base film of the aforementioned amorphous or the first polycrystal semiconductor film so as to prolong the solidification time up to the completion of the solidification by suppressing the heat dissipation from the molten liquid to the substrate.

The method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention comprises irradiating a high energy beam onto a predetermined position of a surface of an amorphous or a first polycrystal semiconductor film to melt the aforementioned semiconductor film, and solidifying the semiconductor film to form a polycrystal, wherein the beam is irradiated to the surface of the semiconductor film so as to form a standing wave, and a heat density distribution which has the same cycle as the standing wave is generated at the predetermined position to melt the semiconductor film.

The method for manufacturing the polycrystal semiconductor film according to the third aspect of the present invention is further characterized in that the standing wave is formed by irradiating at least two laser beams at an incident angle which allows the standing wave to be formed, or by irradiating at least one standing wave at a predetermined angle and in a polarized light state.

Furthermore, the method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention is characterized in that the incident angle is set so that the cycle of the heat density distribution is set to 1 to 10 μm.

Next, the method for manufacturing the polycrystal semiconductor film according to the first aspect of the present invention will be explained.

The process for solidifying the semiconductor film to which the high energy pulse beam is irradiated will be schematically shown in FIGS. 1A, 1B and 1C.

FIG. 1A shows a relation between the laser output and an elapsed time, showing that the laser output rises abruptly. Incidentally, this pulse width is about more than 10 n sec.

FIG. 1B shows a change of the temperature of the semiconductor film with an elapsed of time by the application of the aforementioned pulse beam. Incidentally, the temperature of the semiconductor film rises by the irradiation of the pulse beam with the result that the temperature of the semiconductor film attains the melting point at time To, and the film is in a liquid state. At time Ts, the semiconductor

film is a complete solid state via the state that the solid and the liquid coexist between To and Ts. The solidification time according to the present invention is Ts−To.

FIG. 1C schematically shows a relation between the heat dissipation and the elapsed time.

In other words, the heat dissipation speed D by heat dissipation increases immediately after the start of the beam irradiation, and the heat dissipation speed D attains the peak by the melting of the film (To). The heat dissipation speed D is maintained with the result that a constant heat dissipation speed is maintained until the latent heat amount M of the solid state film becomes equal to the total amount of heat dissipation by passing through the solid and liquid coexisting state (D.T=M, but T refers to a time until the completion of the solidification), and the heat dissipation speed decreases again at the time of the completion of the solidification.

The change in an electrical resistivity of the silicon semiconductor film by the change of the solid and liquid state is shown in FIG. **2**. The axis of abscissa shows a silicon temperature while the axis of ordinates shows a resistivity of the silicon. The silicon changes from the solid to the liquid in the vicinity of 1420° C. and the resistivity lowers from 5×10^{-2} Ω·cm to 1×10^{-4} Ω·cm.

Furthermore, FIG. **3** shows a relation between the impurity concentration in the silicon and the resistivity thereof. With the solid under room temperatures, the resistivity of an n-type silicon having an impurity concentration of $10^{16}cm^{-3}$ is about 1 Ω·cm. In other words, it has been made clear that the ratio of resistivity of the silicon molten part to that of the silicon solid of a high energy beam non-irradiation part (to room temperature) is about $1\times10^{31\ 4}$ Ω·cm: 1 Ω·cm, that is, $1/10000$.

By the way, the heat amount which is generated per unit time in the resistor (R (Ω)) to which rated voltage (E(V)) is applied is set to $Q=I\times E=E^2/R$ (I(Amp) denotes a current which flows through the resistor). Consequently, when the rated voltage is applied to the semiconductor film of the liquid and the solid, it has been made clear that the ratio r of the heat amount which is generated is set to r=s when the ratio of the resistance value of the semiconductor of the liquid and the solid is denoted by s (liquid/solid). In the case of the silicon, since the electric resistance is lower by approximately four digits in the liquid at the melting point as compared with the resistance value of the solid at room temperature, the heat amount of the liquid is 10000 times as large as the heat amount of the solid.

In other words, in the case where the semiconductor film is placed in an appropriate electric field, and a high energy pulse beam is irradiated thereto, only the semiconductor film which is molten with the beam irradiation is effectively heated as compared with the solid part.

Since the heat amount which is generated in proportional to the second power of that of the electric field E, it is possible to control the generated heat amount of the liquid and the solid by selecting an appropriate electric field. Consequently, the silicon in the liquid state can be gradually solidified by setting the heat amount which is generated in the molten liquid to a level slightly smaller than the heat dissipation amount. Thus, the solidification, that is, the time until the silicon is completely solidified can be prolonged with the extended duration of the molten state.

Next, the solidification time T' until the completion of the solidification, which is prolonged by the application of the electric field will be calculated with respect to (1) the case of a rated electric field and (2) the case of the constant heat generation.

(1) In the Case of Constant Electric Field

With respect to the case of the constant electric field, the heat generation of the semiconductor film in the solidification process and the change in temperature is shown in FIG. **4**.

The electric resistance of the molten liquid and the electric resistance of the solid of the semiconductor film are denoted by R1 and R2 respectively, the heat dissipation speed is denoted by D, and the time until solidification is denoted by T'. For the time of the start of solidifying, it is required that heating speed ($E^2/R1$) is smaller than heat dissipation speed D. Consequently, the upper limit of the intensity of the electric field for heating is set to $E^2<(DR1)$. Since the resistance of the semiconductor film rises (R1→R2) corresponding to the formula {(R2−R1)X+R1} [x: solidification rate (0<x<1)], and the heating amount Q abruptly lowers depending on an increase of the solidification rate, the upper limit of time T' until the completion of the solidification, which satisfies the formula M=DT'-Q is two times the solidification time T in the case of the absence of the aforementioned heating means. In other words, in the application of the constant electric field, the time until the completion of solidification can be prolonged two times at most.

It can be seen that since the cooling speed of the semiconductor film in this case is determined by the formula $[D-E^2/\{(R2-R1)X+R1\}]$, the cooling speed increases along with the progress of the solidification.

(2) In the Case of Constant Heat Generation by the Control of the Electric Field.

The case in which the intensity of the applied electric field is controlled so that a constant heat is generated within the solidification time will be explained by using FIGS. **5**A, **5**B and **5**C. Providing that heat dissipation speed at the melting point is constant, the cooling speed of the semiconductor film during the solidification is always constant in the case of constant heat generation. Realizing the condition of the constant heat generation, the change of the intensity of the electric field with the passage of time, time t from the irradiation of the laser beam, and the latent heat amount M of the semiconductor film are calculated from the relation equation of $E^2=(D-M/T')\{(R2-R1)X+R1\}$. The relation between the electric field, the heat dissipation and generation speeds and the change in temperature is shown in FIGS. **5**A, **5**B and **5**C. In other words, when the intensity of the electric field is controlled in the quadratic function in synchronization with the irradiation of the laser beam, an arbitrary solidification time can be obtained, and an arbitrary cooling speed can be obtained.

As a method for generating the electric field in the semiconductor film, an electric heating method or the electromagnetic induction method are available. In the former case, an electric area must be formed inside of the irradiated portion of the high energy beam. In the latter case, only the specimen is placed in the high frequency electric field. Furthermore, since the glass substrate is an insulator and the magnetic permeability is high, the irradiation of the laser beam is not hindered by providing an induction coil on a rear surface where the semiconductor film is not attached.

Furthermore, in both cases, it is possible to arbitrarily set the solidification time and the cooling speed by changing the intensity of the electric field in synchronization with the high energy pulse beam to control the heat amount which is generated within the molten liquid.

Next, a method for manufacturing the polycrystal semiconductor film according to the second aspect of the present invention will be explained.

In the method for manufacturing the polycrystal semiconductor film comprising irradiating a high energy beam onto the surface of the semiconductor film comprising amorphous or first polycrystal material, melting the aforementioned semiconductor film, and further solidifying the film to form the polycrystal film, there can be considered a method of suppressing the heat dissipation on the side of heat dissipation with respect to the method of suppressing the input side of heat.

Generally, as a base film (an undercoat film) of the silicon semiconductor film, SiO_2 film and SiN film are used from the viewpoint of heat resistance property and an impurity barrier. The heat resistance property of both films is sufficient for Si melting, but the thermal conductivity is 0.01 cal/cm.S,.° C. or more at a temperature of 1000° C. or more, hence the heat dissipation to the substrate cannot be sufficiently suppressed to a relatively high level.

As a result of an intensive study, the inventors of the present invention has found that a heat flow speed can be set to ½ to ⅓ by decreasing the thermal conductivity to ½ to ⅓ of the above-mentioned ceramic material, and the solidification time can be prolonged to two to three times.

The film which can be applied as the base film was investigated from the viewpoint of the heat resistance property and the thermal conductive property. It was found that ZrO_2, TiO_2, Y_2O_3, HfO_2, MgO, Ta_2O_3, Nd_2O_3 or the like can be used. As a result of considering an inappropriate properties such as moisture absorption and the lack of transparence as an LCD panel, it was found that ZrO_2, TiO_2, $Y2O_3$, and HfO_2 are an appropriate base film.

In the case where these materials are used as a base film of the semiconductor film, the heat dissipation from the part, which is molten by the irradiation of the high energy beam, to the substrate can be suppressed. The molten state after the irradiation of the laser beam can be maintained for a long time, the solidification time up to the solidification and the polycrystallization is prolonged with the result that a polycrystal semiconductor film having large crystal grains can be manufactured.

Next, the method for manufacturing the polycrystal film according to the third aspect of the present invention will be further explained.

The method for manufacturing the polycrystal semiconductor film according to the third aspect of the present invention comprising the steps of irradiating a high energy beam onto a predetermined position of a surface of an amorphous or a first polycrystal semiconductor film to melt the aforementioned semiconductor film, and solidifying the semiconductor film to form a polycrystal thereby forming a polycrystal film comprising polycrystal grains having a uniform and large diameter is characterized in that the high energy beam is irradiated to the surface of the semiconductor film so as to form a standing wave, and a heat density distribution which has the same cycle as the aforementioned standing wave is generated at the predetermined position to melt the semiconductor film.

As described above, in order to generate large crystal grains in the polycrystal semiconductor film, the control of the density of residual nuclei and the generation position of nuclei is important. However, in the method for manufacturing the polycrystal semiconductor film by means of the conventional excimer laser annealing, the size of the crystal grains which are generated largely changes with a minute change in the intensity of the laser beams in the vicinity of the limit value of the intensity of the laser beams with the result that a polycrystal semiconductor film having an uniform crystal grains cannot be obtained in a stable manner.

In order to solve the aforementioned problem, the following methods have been considered; (1) the method of forming crystal nuclei in advance at the interface between the base film and the semiconductor film, (2) the method of stabilizing the crystal grains at the interface by rendering non uniformity to the interface configuration and the material quality of the base film, (3) the method of promoting the generation of crystal nuclei by adding different kinds of elements or compounds to the interface with the base film, and (4) the method of forming an intensity distribution in the laser beam to form residual nuclei in the low intensity part. Among the aforementioned methods, a further intensive study has been made on the method (4) which is regarded as the most excellent in terms of an inferior influence to the property of the TFT element and cost thereof.

As the method (4) for forming an intensity distribution of the laser beam, several methods were considered. In other words, the following methods were considered; (a) the method of severing part of the beam, (b) the method of overlapping the positions of the plurality of beams by slightly shifting the positions thereof, and (c) the method of interference by means of diffraction element such as slit or the like. All these methods were insufficient as a method for controlling the crystal nuclei.

Time (solidification time) up to the cooling and solidifying of the semiconductor film which is molten with the pulse laser of more than 10 n sec such as an excimer laser which is used with respect to the polycrysal semiconductor film is extremely short (about 100 n sec), and the maximum grain diameter which can be grown during this period is limited to only several μm. Therefore it is necessary to form the distribution of the residual grains to several μm or less.

Consequently, the cyclic property of the laser beam intensity distribution becomes thousand times or more (more than 10 μm) of the wavelength of light (more than 100 nm) so that the aforementioned condition cannot be satisfied. By a further intensive study, the inventors of the present invention have succeeded in realizing the light intensity distribution having a cycle of several μm by irradiating beam so as to form a standing wave on the surface of the amorphous or the first polycrystal film and in forming a polycrystal film comprising uniform and large crystal grains on the order of several μm by controlling the residual nuclei located at the interface with the base film in a cycle of several μm.

A first method for forming a standing wave in the method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention, two laser beams are irradiated to the predetermined position of the surface of the amorphous or first polycrystal semiconductor film at an incident angle which allows the formation of the standing wave so that a heat density distribution having the same cycle as the standing wave is generated at the aforementioned predetermined position to melt the film.

In other words, by allowing two laser beams to be interfered with each other on the surface of the semiconductor film the standing wave is formed. Then the cycle of the standing wave can be represented by $\lambda/(2\sin\theta)$ wherein λ denotes a wavelength of the laser beam, and θ denotes an incident angle.

Consequently, it becomes possible to control the cycle of the heat density distribution which is formed on the semiconductor film or the cycle of the standing wave in a high precision by adjusting the incident angle.

Here, in the TFT-LCD polysilicon, it is desired that the grain diameter of the polysilicon is set to 1 to 10 μm. However, in order to form the polysilicon film having the grain diameter of this size, it is desired that the incident

angle is 0.7 degrees or more and 8.2 degrees or less when the wavelength of the laser beam is set to 230 to 280 nm, the incident angle is set to 0.9 or more and 8.9 or less degrees when the wavelength of the laser beam is set to 280 to 400 nm, the wavelength thereof is set to 1.5 or more and 15 degrees or less when the laser beam is set to 400 to 800 nm, and the wavelength thereof is 2.9 or more to 30 degrees or less when the wavelength thereof is set to 800 to 1200 nm.

The second method for forming the standing wave in the method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention comprises applying at least one laser beam to a predetermined position of the surface of the amorphous and polycrystal semiconductor at a predetermined incident angle and in a polarization state to form a standing wave, and generating a heat density distribution in the same cycle as the standing wave to melt the semiconductor film.

In this method, the standing wave is formed on the surface of the aforementioned semiconductor film by irradiating again a second laser beam on to a rough surface roughness, the rough surface being formed after the semiconductor film is once molten and recrystallized with a first irradiation of the laser beam, wherein scattering beams generated on the rough surface are interfered with each other.

Here, it is at least required that the polarization state of the laser beam forms an angle other than 45 degrees with respect to the reflection surface, and it is further desired that the polarization state stand in a parallel state (P polarization) or a vertical state (S polarization). Then either a parallel state or a vertical state is provided, with respect to the cycle of the standing wave the standing wave having a cycle of $\lambda/(1-\sin\theta)$ and $\lambda/(1+\sin\theta)$ is generated in a direction vertical to the polarization direction, and a standing wave having a cycle of $\lambda/\cos\theta$ is generated in a direction parallel to the polarization direction.

In particular, the standing wave having a cycle of $\lambda/(1 \sin+\sin\theta)$ is strong in the condition approximate to the vertical direction of 35 degrees or less. On the other hand, the standing wave a cycle of $\lambda/\cos\theta$ is allowed to be incident in a slanting manner at an angle of 35 degrees or more, and the standing wave is strong in the polarization state parallel to the reflection surface, that is, the P polarization.

Consequently, it becomes possible to control the cycle of the standing wave, or the cycle of the heat density distribution which is formed on the surface of the semiconductor film.

Incidentally, in this case, in order to form the polysilicon film having a diameter of 1 to 10 μm, the incident angle is set to 76 degrees or more and 88.6 degrees or less when the wavelength of the laser beam is 230 to 280 nm, it is desired that the incident angle is set to 72 degrees or more and 88.2 degrees or less when the wavelength of the laser beam is 280 to 400 nm, it is desired that the incident angle is set to 59 degrees or more and 87.1 degree or less when the wavelength of the laser beam is 400 to 800 nm, and the incident angle is set to 0 degree or more and 84.3 degrees or less when the wavelength of the laser beam is set to 800 to 1200 nm.

The summary of the invention has been described with respect to the method of manufacturing the polycrystal semiconductor film according to the first, second and third aspect of the invention, the advantage of the invention can be further heightened by combining these methods.

In other words, in the methods according to the first and the second aspect of the invention, the time of solidification the semiconductor film can be prolonged by irradiating the high energy pulse laser. In other words, the method contributes to the prolongation of the solidification time.

Furthermore, in the method for manufacturing the semiconductor film according to the third aspect of the invention, the uniformity in the size of the crystal grains can be remarkably improved by controlling the interface crystal nuclei using the interference of the laser beams.

Embodiments of the invention will be described in detail hereinbelow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A, FIG. 1B and FIG. 1C are views for generally explaining a process of melting and solidifying the semiconductor film by a laser under a non-electric field. FIG. 1A shows a relation between a laser output and time. FIG. 1B shows a relation between the semiconductor film temperature and time. FIG. 1C shows a relation between heat dissipation speed and time.

FIG. 2 is a view showing a temperature change of an electric resistivity of Si which is a semiconductor film material.

FIG. 3 is a view showing a relation between an impurity concentration in Si and the electric resistivity (room temperature).

FIG. 4A, FIG. 4B and FIG. 4C are views for generally explaining a process of melting and solidifying the semiconductor film by a laser under a constant electric field. FIG. 4A shows a relation between the voltage and the time. FIG. 4B shows a relation between heat dissipation speed, heating speed and time. FIG. 4C shows a relation between the semiconductor film temperature and time.

FIG. 5A, FIG. 5B, and FIG. 5C are views for generally explaining a process of melting and solidifying the semiconductor film by a laser under a control of the electric field (constant heat generation). FIG. 5A shows a relation between the voltage and time. FIG. 5B shows a relation between heat dissipation speed and heating speed. FIG. 5C shows a relation between the semiconductor film temperature and time.

FIG. 6A and FIG. 6B are views showing an arrangement of a laser application device and an induction heating device for explaining a method for manufacturing a polycrystal semiconductor film according to a first aspect of the present invention, FIG. 6A is a perspective view, and FIG. 6B is a sectional view.

FIG. 7A and FIG. 7B are views showing an arrangement of the other laser application device and an electric heating device for explaining the polycrystal semiconductor film according to the first aspect of the present invention, FIG. 7A is a perspective view, and FIG. 7B is a sectional view.

FIG. 8 is a sectional view for explaining a heat stream by heat radiation immediately after heating by laser beam irradiation the base film and the semiconductor film which are formed on the substrate in the method for manufacturing the polycrystal semiconductor film.

FIG. 9 is a view illustrating a cross section structure of the substrate in which ZrO_2 film is used as a base film in the method for manufacturing the polycrystal semiconductor film according to the second aspect of the present invention.

FIG. 10A is a view for explaining one example of a position relation (optical arrangement) of laser light and the semiconductor substrate.

FIG. 10B is an enlarged view of an A part shown in FIG. 10A.

FIG. 11 is a view showing a relation between an incident angle formed between two laser beams and the semiconductor film and a cycle of a standing wave which is formed on the surface of the semiconductor film.

FIG. **12** is a front view showing a position relation (optical arrangement) between other laser light and the semiconductor substrate in the method for manufacturing the polycrystal semiconductor film according to a third aspect of the present invention.

FIG. **13** is a front view showing a position relation (optical arrangement) between still the other laser light and the semiconductor film in the method for manufacturing the polycrystal semiconductor film according to the third aspect of the present invention.

FIG. **14** is a view showing a relation between an incident angle formed between the laser beam and the semiconductor substrate and a cycle of a standing wave formed on the surface of the semiconductor film.

FIG. **15**A and FIG. **15**B are views showing a position relation (optical arrangement) in the method for manufacturing the polycrystal semiconductor film according to the third aspect of the present invention, FIG. **15**A is a front view and FIG. **15**B is a plan view.

FIG. **16** is a view schematically showing a method for manufacturing a conventional polycrystal semiconductor film.

FIG. **17** is a view schematically showing a manufacturing method according to a second aspect of the invention.

FIG. **18** is a view schematically showing a combination of the manufacturing method according to a first aspect of the invention and the manufacturing method according to a second aspect of the invention.

FIG. **19** is a view schematically showing a combination of the method for manufacturing the polycrystal semiconductor film according to the first, the second and the third aspects of the present invention.

PREFERRED EMBODIMENT OF THE INVENTION

Forms for embodying the present invention will be explained hereinbelow.

Embodiment 1

In the beginning, an embodiment of a method for manufacturing the polycrystal semiconductor film according to a first aspect of the invention will be described.

FIG. **6** is a schematic view showing an arrangement of a laser application device and an electromagnetic induction heating device for embodying the method for manufacturing the polycrystal semiconductor film according to a first aspect of the invention. A high energy beam **1** (an excimer pulse laser is used in this embodiment) from a single light source is vertically applied to a semiconductor film **9** on a glass substrate **7**. An induction heating coil **4** is arranged on a rear surface of the glass substrate of the high energy beam application part. A high frequency current flows through a coil from a high frequency electric source **5** with the result that the substrate itself moves in synchronization with a high energy pulse beam so that a high energy beam can be irradiated to the substrate itself and the substrate can be induction heated.

A resistance value of the a melting part **6** of the semiconductor film, which is generated by the irradiation of the high energy beam, is lowered so that an eddy current flows through the semiconductor film with an alternate current field, which is generated in the semiconductor film, and only the melting part is induction heated with the result that the solidification time is prolonged.

It is required that a heat generation speed from the induction heating does not raise the temperature of the melting part, that is the heat generation speed is smaller than the heat dissipation speed for gradually solidifying the silicon in the liquid state. It is required that the high frequency electric field and a high frequency is set so that the heating amount at this time does not exceed the heat dissipation speed because the resistance value becomes lowest in the state in which the application part is completely molten.

The solidification time can be prolonged by two times at most by the high frequency induction heating of the constant output of such constant voltage with the result that the grain diameter of the crystal grains which can be grown within this solidification time can be enlarged by approximately two times and the TFT element properties such as mobility can be improved.

Furthermore, the voltage and the frequency of the high frequency induction are controlled in synchronization with the irradiation of the high energy beam, and the lowering of the heating efficiency is compensated with an increase in the resistance value accompanying with the progress of solidification of the semiconductor film and the constant heated state can be kept during the solidification time with the result that an arbitrary solidification time can be selected and more larger crystal grains can be grown.

Incidentally, the high frequency zone which can be used in the present invention can be used during the scope of 1 KHz to 1 GHz. In the case of the control of the electric field, it is desirable that a frequency zone of 100 MHz or more (one cycle: 10 n sec) can be used wherein a response is possible which is sufficiently fast as compared with the solidification time of about 100 n sec.

Furthermore, a micro-wave of 1 GHz or more is applied to a high energy beam by using a wave guide path, an advantage similar to the induction heating (micro-wave heating) can be obtained.

Embodiment 2

Another embodiment of the method for manufacturing the polycrystal semiconductor film according to the first aspect of the present invention will be described hereinbelow.

FIG. **7** is a schematic view showing an arrangement view of the laser application device and the electric heating mechanism for realizing the polycrystal semiconductor film according to the present invention. A high energy beam (an excimer pulse laser beam is used in the present invention) is irradiated to the semiconductor film **9** on the glass substrate **7** vertically from a single light source. On or beneath the semiconductor film located at both ends of the long side of the high energy beam irradiation part, metal wirings **17** and **18** such as Al and the like is formed in such a manner that the metal wirings cross the substrate, and a voltage is applied to the wirings from the power source **19**.

By irradiating a high energy beam to the semiconductor film between electrodes including the electrodes, the semiconductor film is molten and the resistance value of the semiconductor film is lowered so that current flows through the molten part **6** of the semiconductor film and the molten semiconductor film itself is resistance-heated.

Since this heat amount is proportional to the second power the voltage which is applied, the voltage can be controlled. In the case of the constant voltage, it is required that the heating speed is smaller than the heat dissipation speed under the melting point. In other words, it is required that the voltage is set in accordance with $D>(E^2/R_L)$. Furthermore, it is possible to prolong the solidification time to an arbitrary length by controlling the voltage in synchronization with the high energy pulse beam to compensate the lowering of the heating amount caused by the rise in the resistance value accompanying with the progress of the solidification of the semiconductor film.

As described above, in accordance with the present invention, there is an advantage in that in the process of manufacturing the polycrystal semiconductor film by melting and crystallizing the semiconductor film, the solidification time can be arbitrarily prolonged irrespective of the length of the pulse of the pulse laser with the result that the polycrystal with a large grain diameter can be stably manufactured, and the crystal property of the polycrystal semiconductor film and the TFT property can be improved.

Embodiment 3

In embodiment 3, the method for manufacturing the polycrystal semiconductor film according to the second aspect of the present invention will be explained by referring to FIG. **8**.

In the polycrystal Si film formation specimen comprising three layer structure of the semiconductor film **9** the base film **10** and the glass substrate **7** shown in FIG. **8**, a ZrO_2 sputtering film is used as the base film. Furthermore, for comparison, a specimen in prepared in which the conventional SiO_2 film is used as the base film. The apparatus shown in FIG. **6** is used except for the electromagnetic induction heating device. After the XeCL excimer laser is irradiated 10 times at the optimal fluence of 300 mJ/cm^2, the average grain diameter of the polycrystal silicon film and the minimum grain diameter were compared. The result is shown in Table 1.

TABLE 1

Grain Diameter of the Polycrystal Silicon Film

Kind of Base Film	Average Grain Diameter of Polycrystal Silicon Film	Minimum Grain Diameter
SiO_2	500 nm	50 nm
ZrO_2	1000 nm	65 nm

As shown in Table 1, in the case where the same condition laser is applied, it has been recognized that the average grain diameter is enlarged to two times by using ZrO_2. In other words, it is judged that the solidification time is prolonged, thereby the grain diameter being enlarged.

As described above, in the process of manufacturing the polycrystal semiconductor film by melting and crystallizing the semiconductor film by the high energy pulse laser, time up to the solidification can be prolonged, and the polycrystal semiconductor film having a large grain diameter can be manufactured stably with the result that the crystal property and the TFT property of the polycrystal semiconductor film can be improved.

Embodiment 4

In the embodiment, the method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention will be explained by referring to FIGS. **10A** and **10B**.

FIG. **10A** is a view showing a position relation between the laser beam and the semiconductor film. FIG. **10B** is an enlarged view of an A part shown in FIG. **10A**. In FIGS. **10A** and **10B**, reference numeral **7** denotes a glass substrate, and 9 an amorphous semiconductor film or a first polycrystal film. As shown in FIG. **10A**, the laser beam **1** is split into two beams with a beam splitter **3***a*. Then the two split beams are allowed to be intersected and interfered so that a standing wave having the cycle of the wavelength order (on the order of μm) is formed on the surface of the semiconductor film **9**.

For example, in the case where the wavelength of the laser beam 1 is λ, as shown in FIG. **10B**, the cycle of the standing wave formed on the surface of the semiconductor film **9** is set to $\lambda/(2\sin\theta)$ (for example, refer to Appl. Phys. Lett. 57, 132, 1990). Then, with the intensity distribution, the heat generation density distribution having the same cycle with the aforementioned standing wave is formed on the surface of the semiconductor film **9**. In a low part of the heat generation density distribution corresponding to the valley (knot part) of the standing wave, the residual nuclei can be controlled on the order of the wavelength (on the order of μm). As a consequence, a polycrystal semiconductor film which has uniform large crystal grains can be manufactured.

FIG. **11** is a view showing a relation between the incident angle θ with respect to two beams semiconductor film **9** shown in FIG. **10B** and the cycle of the standing wave which is formed on the surface of the semiconductor film **9**. It can be seen that when the incident angle θ is not more than 30 degrees, the standing wave having the cycle of the wavelength of λ or more of the laser beam can be formed whereas when the incident angle θ is not less than 30 degrees the standing wave having the cycle of the wavelength of λ or less can be formed.

In this manner, according to embodiment 4, the cycle of the standing wave can be controlled with the incident angle θ. Consequently, the incident angle θ may be set to the scope of 5 to 20 degrees as shown in FIG. **11** in order to set the cycle of the interference fringe pattern to about several times of the wavelength λ of the laser beam **1**.

For example, in the polysilicon for TFT (thin film transistor)—LCD (liquid crystal display), it is desired that the grain diameter is set to 1 to 10 μm. In order to manufacture the polysilicon having this diameter in the method for manufacturing the polycrystal semiconductor film, the relation between the wavelength λ of the laser beam **1** and the incident angle θ is shown in Table 2.

TABLE 2

Relation between the Wavelength λ of the laser beam 1 and Incident Angle θ

Wavelength λ of the laser beam 1	Incident Angle θ
KrF laser (248 nm)	$0.7° \leqq \theta \leqq 8.2°$
XeCl laser (308 nm)	$0.9° \leqq \theta \leqq 8.9°$
Ar^+ laser (514.5 nm)	$1.5° \leqq \theta \leqq 15°$
YAG laser (1060 nm)	$2.9° \leqq \theta \leqq 30°$

Incidentally, in order that the heat generation density distribution which is generated on the surface of the semiconductor film **9** with the aforementioned standing wave forms residual nuclei, the heat generation density at the valley part (knot part) of the standing wave (Q_{Bottom}) must be 0 or more and not less than the heat amount Q_1 necessary for the complete melting of the semiconductor film **9**. On the other hand, the heat generation density (Q_{Top}) at the peak part of the standing wave must be not less than Q_L and not more than the heat density amount Q_{AB} at which the semiconductor film **9** is ablated (the temperature of the semiconductor film exceeds the melting point by absorbing heat and is vaporized).

In other words, the following equation (1) must be satisfied so that the residual nuclei are stably formed on the valley part (knot part) of the standing wave.

$$0 \leqq Q_{Bottom} \leqq Q_L \leqq Q_{Top} \leqq Q_{AB} \quad (1)$$

Here, when the average output $(Q_{Top}+Q_{Bottom})/2$ is set to Q_L, the following relation can be calculated from the aforementioned equation (1) providing that $\pm\delta$ represents the

change rate of the laser beam output 1, $Q_{P\text{-}P}(=Q_{Top}-Q_{Bottom})$ denotes a difference between the heat generation density at the valley part and at the peak part.

$$Q_{P\text{-}P} \geq 2\delta Q_L \quad (2)$$

It can be seen from the equation (2) that a difference in the heat generation density distribution $Q_{P\text{-}P}$ of the standing wave, namely the amplitude must be set to not less than the change in the output of the laser beam.

However, as a factor which affects the existence of the residual nuclei, the change in the output of the aforementioned laser beam is a main factor. As other factors, the change in the thickness of the semiconductor film and the change in the thermal conductivity of the base film can be given. Consequently, the amplitude must be set to a level more than the total fluctation.

Incidentally, in the embodiment, one laser beam is split, but the present invention is not limited thereto. As long as the wavelengths and the phases thereof agree with each other, two or more laser beams may be combined to be used.

Embodiments of the present invention will be further explained.

Embodiment 5

Embodiment 5 relates to the method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention, but embodiment 5 has a different optical arrangement with embodiment 4.

FIG. **12** shows an optical arrangement which is different from embodiment 4.

In the apparatus according to embodiment 4, excimer laser beam **11** is vertically irradiated to the surface of the silicon film on the glass substrate **7**. On the other hand, second laser beam **13** which has a longer wavelength (λ) than the excimer laser beam **11** is split into two beams by using a beam splitter **3***b* so that each of the beams is irradiated to an excimer laser application part of the silicon film **9** at an incident angle θ by using reflection mirrors **5***c*, **5***d* and **5***e* so as to allow the two beams to be interfered with each other and a standing wave is formed on the silicon film **9**.

Then the heating by the excimer laser beam **11** and beam the heating by the standing wave which is formed by the second laser beam **13** forms a temperature distribution having a cycle of $\lambda/(2\sin\theta)$.

At this time, when the output of the excimer laser beam **11** and the second laser beam **13** are set so that the low temperature part of this temperature distribution becomes not more than the melting point (1415° C.) and the high temperature part of the temperature distribution part becomes not less than the melting point of the silicon, the residual nuclei can be selectively formed only on the low temperature part of the standing wave.

Then by using the residual nuclei as a seed of the crystal grains after that, the crystal having a large grain diameter can be formed.

When the glass substrate as a whole is moved at a step less than the width of the laser beam at each time of laser beam application, the silicon film as a whole can be recrystallized.

Embodiment 6

Embodiment 6 relates to the method for manufacturing the polycrystal semiconductor film according to the third aspect of the invention, but embodiment 6 has a different optical arrangement with embodiments 4 and 5.

FIG. **13** shows an optical arrangement of the laser beam application apparatus according to embodiment 5.

In this apparatus, the excimer laser beam **11** is vertically irradiated to the surface of the silicon film **9** on the glass substrate **7**. On the other hand, the second laser beam **13** having a longer wavelength (λ) than the excimer laser beam **11** is split into two beams by using the beam splitter **3***c* so that each of the laser beams is irradiated from the rear surface of the glass substrate **7** at an incident angle θ on the excimer laser application part of the silicon film **9** by using reflection mirrors **5***f* and **5***g* so that the two beams are allowed to be interfered with each other and the standing wave is formed on the silicon film **9**.

In this manner, an object of allowing the second laser light **13** to be incident from the rear surface of the glass substrate **7** is to prevent the silicon particles which jump out by heating from colliding with the optical system such as the reflection mirrors **5***f* and **5***g*.

At this time, when the outputs of the excimer laser beam **11** and the second laser beam **13** are set so that the low temperature part of this temperature distribution becomes not more than the melting point (1415° C.) and the high temperature part of the silicon becomes not less than the melting point, the residual nuclei can be formed only on the low temperature part of the standing wave.

Then, a crystal having a large grain diameter can be formed by forming the residual nuclei as a seed of crystal growth.

Incidentally, when the glass substrate as a whole is moved at a step not more than the beam width of the laser light at each time of laser application, the silicon film as a whole **9** can be recrystallized

Embodiment 7

Embodiment 7 relates to a method for manufacturing the polycrysal semiconductor film according to the third embodiment of the present invention. Unlike embodiments 4 through 6, two laser beams is not allowed to intersect and to be interfered with each other so that the standing wave is formed on the surface of the semiconductor film. In embodiment 7, one laser beam in a straight line polarization state which is either parallel or vertical to the reflection surface is allowed to be slantly incident on the semiconductor film so that a standing wave having a cycle on the wavelength order (μm) on the surface of the semiconductor film with the interference of the surface scattered beam.

Then, like embodiments 4 through 6, the heat generation density distribution is formed which has the same cycle as the standing wave on the semiconductor film. At a low part of the heat generation density distribution corresponding to the valley part (knot part) of the standing wave, the melting of the nuclei is stabilized, the residual nuclei are controlled on the order of the wavelength (μm order) thereby making it possible to manufacture a polycrystal semiconductor film having a large crystal grain.

In the formation of the standing wave according to the embodiment, the surface roughness, which is formed after the melting and the recrystallization of the semiconductor film by the irradiation of the laser beam, becomes the starting point of the light scattering (light split).

The surface roughness basically arises from the density change in the solid-liquid state so that it can be considered that an uneven state is formed at the end of the solidification in the case where the solidification proceeds in a lengthwise direction and the crystal nuclei are grown.

Then, when the laser beam is again irradiated to the rough surface of this semiconductor film, the scattered beams which are scattered at the uneven part interferes with each other, and a standing wave is formed on the surface of the film. Consequently, at the multiple time irradiation, an uneven pattern having a specific cycle is finally formed during the repetition of this process (refer to J. Sipe, J. F.

Young, J. S. Perston, and H. M. van Driel, Phys, Rev. B 27, 1141, 1155, 2001, 1983).

Incidentally, according to the aforementioned documents, it has been confirmed that although the polarization state of the laser beam and the form of the standing wave which is generated on the surface of the semiconductor film widely change, a standing wave having a cycle of $\lambda/(1-\sin\theta)$ and $\lambda/(1+\sin\theta)$ is basically generated in a direction vertical to the polarization direction and a standing wave having a cycle of $\lambda/\cos\theta$ is basically generated in a direction parallel to the polarization direction.

In particular, it is known theoretically and experimentally that the standing wave having a cycle of $\lambda/(1+\sin\theta)$ is strong under a condition of the incident angle of vertical state of 35 or less, and that the standing wave having a cycle of $\lambda/\cos\theta$ is strong under a condition of the inclined incident angle of 35 or more and under a parallel polarization state to the reflection surface, that is, the P polarization.

FIG. **14** shows the relation between the incident angle and the standing wave formed on the surface of the semiconductor film.

In FIG. **14**, in the standing wave having a cycle of $\lambda/(1\pm\sin\theta)$, which is strong under a condition of the incident angle of near vertical state, a cycle of $\lambda/(1-\sin\theta)$ which is longer than the wavelength of the laser beam and a cycle of $\lambda/(1+\sin\theta)$ which is shorter than the wavelength of the laser beam are overlapped. On the other hand, the standing wave having a cycle of $\lambda/\cos\theta$ which is strong under a condition of the inclined incident angle and P polarization has a single cycle longer than the wavelength of the laser beam.

Since uniform crystal grains can be formed when the standing wave is uniform, it is desirable that the standing wave having a single cycle of $\lambda/\cos\theta$ is formed.

Here, in order to manufacture the polysilicon for TFT-LCD having a grain size of 1 to 10 μm the polycrystal semiconductor film according to the embodiment of the invention, the relation between the wavelength λ of the laser light and the incident angle $\theta$is shown in Table 3.

TABLE 3

Relation between Wavelength λ of Laser Beam and Incident Angle θ

Wavelength λ of Laser Beam	Incident Angle θ
KrF laser (248 nm)	$76° \leqq \theta \leqq 88.6°$
XeCl laser (308 nm)	$72° \leqq \theta \leqq 88.2°$
Ar^+ laser (514.5 nm)	$59° \leqq \theta \leqq 87.1°$
YAG laser (1060 nm)	$0° \leqq \theta \leqq 84.3°$

Incidentally, the amplitude of the standing wave to be formed is determined from the polarizing degree of the incident laser beam and the incident angle thereof, and the optical constant and the surface form of the semiconductor film. Among them, although the polarizing degree, the incident angle, and the optical constant can be easily determined, but with respect to the surface form, it is difficult to determine for change and formation thereof during the repetition of the laser beam irradiation. Furthermore, along with the change and formation of the surface form, an intensity of the standing wave to be formed increases along with the change and formation of the surface form. Therefore, it is not easy to estimate the amplitude (intensity) of the standing wave.

Therefore, a constant surface form can be formed at a fewer irradiation times as the polarizing degree is higher.

As a consequence, a high polarizing degree is desirable for the formation of a strong standing wave. At least 10% polarizing degree is required, and more preferably, 90% or more is required.

In the aforementioned embodiment, an excimer laser single beam can be used as the second laser beam. However, the excimer laser beam is controlled with a high precision with respect to the shaping of the beam configuration, and uniformity thereof. Therefore, it is extremely difficult to control the incident angle. Consequently, other than the excimer laser, the second laser beam is separately provided which has a longer wavelength than the wavelength (200 to 400 nm), and the laser beam is irradiated in an overlapping manner to the application part of the excimer laser beam, and a standing wave having an arbitrary cycle can be formed on the semiconductor film by controlling the wavelength, the polarizing degree and the incident angle of the aforementioned second laser beam.

FIGS. **15A** and **15B** are views showing an optical arrangement of the laser beam apparatus for embodying the method for manufacturing the polycrystal semiconductor film according to the embodiment of the present invention.

FIG. **15A** is a front view thereof, and FIG. **15B** is a top view thereof.

In this apparatus, the excimer laser beam **11** is vertically irradiated to the surface of the silicon film **9** on the glass substrate **7**. On the other hand, the second laser beam **15** which is a long wavelength light and a linear polarization is applied to the irradiation part of the excimer laser beam **11** of the silicon film **9** in the P polarization state. In the case where the excimer laser beam **11** is irradiated a plurality of times to repeat the melting and recrystallization of the silicon film **9**, at the incident angle θ of the second laser light is $0° \leqq \theta \leqq 35°$ uneven configuration having a cycle of $1/(1-\sin\theta)$ and $1/(1+\sin\theta)$ is formed on the surface of the silicon film **9** in a vertical direction with respect to the polarizing direction. Furthermore, in the case of $35° \leqq \theta$, an uneven configuration having a cycle of $1/\cos\theta$ is formed on the surface of the silicon film in a direction vertical to the polarizing direction. As a consequence, the standing wave having the same cycle can be formed.

Then the heat generation density distribution having the same cycle is formed with this standing wave. Residual nuclei are formed at valley portions of this standing wave, and the residual nuclei are used as a seed of the crystal growth to be recrystallized with the result that a polysilicon film having an even and large grain diameter can be formed.

Incidentally, the total output of the two laser beams to be applied is set to a value less than the output at which the silicon film **9** is completely molten. At the same time, in the case where the output of the second laser beam **15** must be 1000/F % or more when the polarizing degree is denoted by F % (F>10). This is because it is necessary to have a polarizing degree of 10% or more with respect to the total output of laser.

As explained above, according to the method according to the third aspect of the present invention, when the semiconductor film is molten and recrystallized by the irradiation of the high energy pulse laser to form the polycrystal semiconductor film, the distribution of the residual nuclei which are present in the interface is controlled on an order of μm so that the stabilization of distribution can be obtained. Thus, the polycrystal semiconductor film having an even and large grain diameter can be obtained steadily. Consequently, the crystallinity of the polycrystal semiconductor film and the property of TFT element using the polycrystal semiconductor film can be improved.

Embodiment 8

With respect to the method for manufacturing the polycrystal semiconductor film according to the first, the second

and the third aspect of the invention, a general comparison will be explained in which the method is individually executed and all the methods are executed in combination with each other.

Embodiment 8 will be explained with respect to FIGS. **16**, **17**, **18** and **19**.

FIG. **16** is a view for explaining a conventional method for manufacturing the polycrystal semiconductor film, showing an apparatus for melting, solidifying and forming the polycrystal film by applying excimer laser onto the glass substrate, and the surface of the amorphous silicon film (a-Si film) which is formed on the SiO_2 base film provided thereon.

FIG. **17** is a view for explaining the method corresponding to the embodiment 3 (the method according to the second aspect of the present invention). In the place of the conventional SiO_2 base film, ZrO_2 film is used as the base film.

FIG. **18** is a view showing the method for manufacturing the polycrystal semiconductor film according to the first aspect of the invention in which the heating of the high frequency induction heating is added to the heating of the semiconductor film molten part in addition to the conventional method for manufacturing the polycrystal semiconductor film, or the method according to the second aspect of the present invention shown in FIG. **17**.

FIG. **19** is a view showing a method in which the control of the interface crystal nuclei which is included in the method according to the third aspect of the invention is added to the aforementioned FIG. **18**.

In other words, the advantage of enlarging the crystal grain diameter is compared with respect to the case of using the base film as the base film, the case of induction heating, and the case of controlling the crystal nuclei with the laser interference method.

Specifically, the XeCl excimer laser (having a pulse width of 20 nano second) is irradiated to the a-Si film (50 nm) on the SiO_2 base film (200 nm) on the glass substrate at 350 mJ/cm^2. The measurement result of the polysilicon grain diameter distribution is shown in Table 4 with respect to the case of forming the polysilicon film by the conventional method shown in FIG. **16**, the case of using the heat insulating $Zr0_2$ film (200 nm) (FIG. **17**), the case of heating the semiconductor film with the electromagnetic heating (FIG. **18**) and the case of controlling the crystal nuclei with the laser interference method (FIG **19**).

In the case of using the ZrO_2 base film, and in the case of heating the semiconductor film by electromagnetic heating, the optimal output of the excimer laser is 350 mJ/cm_2, and in the case of the laser interference method, the laser output before beam split has become 400 mJ/cm_2.

In the case of ZrO_2 film, the solidification time until the completion of the solidification in the case of heating the semiconductor film by electromagnetic induction will be as follows. In the case of measuring the solidification time by means of measuring the reflection rate by means of He—Ne laser, 100 nano sec is given in the case of using only SiO_2 film, whereas the solidification time can be prolonged to 150 nano sec by replacing the SiO_2 film with ZrO_2 film. Furthermore, in the case of heating the semiconductor film with a high frequency heating of 1MHz·5kW, the solidification time can be prolonged to approximately 200 nano sec. Furthermore, in the case of solidifying the semiconductor film with ZrO_2 base film, the solidification time can be prolonged to 250 nano sec.

Furthermore, in addition to the solidification time, in order to control the crystal nuclei distribution which reside at the interface with the base film, the solidification time does not change in the case of changing the interference width from 300 nm, 600 nm, and 1200 nm at an incident angle of the excimer laser.

As apparent from Table 4, in the case of using ZrO_2 base film and in the case of heating by the electromagnetic induction heating method, the maximum crystal grain diameter of polysilicon is enlarged together with the prolongation of the solidification time. However, in the case where the crystal nuclei distribution are not controlled, a large enlargement of the minimum diameter of crystal grains cannot be recognized.

In contrast, in the case where the interface crystal nuclei distribution is controlled using the laser interference method together with the solidification time prolongation method, it can be seen that the minimum grain diameter becomes close to the maximum grain diameter (the grain diameter distribution becomes narrow), by setting the distance between crystal nuclei to not exceed the maximum grain diameter which is determined by the solidification time. However, in the case of setting the distance between nuclei to exceed the maximum grain diameter determined by the solidification time, the crystal growth from the crystal nuclei does not overtake and supercooling state is generated, thereby fine crystals being generated.

Since the electric property of cross section panel such as TFT-LCD or the like is adjusted according to the lowest property part, the minimum grain diameter of the crystal grains determines the properties of panel. Consequently, in order to manufacture a high property TFT-LCD polysilicon, it is necessary to form polysilicon having a large grain diameter and a narrow distribution of grain diameter. As a material which satisfies the aforementioned condition, a method is desired which includes forming the crystal nuclei distance which is equal to the grain diameter which can be grown within the solidifying time with the laser interference method in addition to the solidification time which is sufficiently prolonged by using ZrO_2 base film, or by electromagnetic heating.

TABLE 4

Prolongation of Solidification Time	Kind of Base Film	SiO_2	ZrO_2	SiO_2	ZrO_2
	Presense of Induction Heating	none	none	present	present
Solidification Time (nano second)		90 to 110	140 to 150	190 to 220	240 to 260
Distribution Control of Crystal Nuclei		Distribution nm)			
	none	50 to 330	165 to 650	180 to 900	100 to 1200
		present			
	Interference Width 300 nm	260 to 320	280 to 310	280 to 310	290 to 310
	Interference Width 600 nm	60 to 330	500 to 610	550 to 630	550 to 650
	Interference Width 1200 nm	55 to 320	60 to 660	90 to 910	1100 to 1250

As described above, in embodiment 8, it has been confirmed that the crystal grains can be uniformed and the size of the crystal grains can be enlarged by using the first, the second and the third methods in combination with respect to the method for manufacturing the polycrystal semiconductor film of the present invention.

As described above, the solidification time to the end of the solidification can be prolonged up in the process of manufacturing the polycrystal semiconductor film by melting, solidifying and crystallizing the semiconductor film by the irradiation of the high energy pulse laser, and the polycrystal semiconductor film having a large and uniform grain diameter can be manufactured by controlling the distribution of the residual nuclei which is present at the interface at the time of melting with the result that an attempt can be made to improve the crystallinity of the polycrystal semiconductor film and the TFT element using the semiconductor film.

What is claimed is:

1. A method for forming a polycrystal semiconductor film comprising the steps of:

irradiating a high energy pulse beam onto a surface of a semiconductor film comprising an amorphous or first polycrystal semiconductor formed on a first surface of a substrate to melt only the semiconductor film; and

solidifying and forming the semiconductor film comprising a polycrystal with a large crystal grain diameter by passing through a solid-liquid coexisting state;

wherein only a liquid part generated by melting the semiconductor film is heated by using a difference in an electric resistance between a solid part and a liquid part in the solid-liquid coexisting state so as to prolong a solidification time until the completion of the solidification of the semiconductor film which has been molten; and

wherein the molten part is heated with the electromagnetic induction heating, the induction heating being carried out by supplying a high frequency current to an induction heating coil provided on a second surface of the substrate to generate an alternate current in the semiconductor film.

2. The method for manufacturing the polycrystal semiconductor film according to claim 1, wherein a heat generation speed by the induction heating is lower than a heat dissipation speed to the substrate from the semiconductor film.

3. The method for manufacturing the polycrystal semiconductor film according to claim 1, wherein an electric field or a frequency is controlled for heating the semiconductor film with electromagnetic induction in synchronization with the high energy pulse beam irradiation, the heating of the electromagnetic induction heating being corrected in correspondence to a high resistance of the semiconductor film accompanying with the change of the ratio of the solid and the liquid during the progress of the solidification, with a constant heat generating state.

4. The method for manufacturing the polycrystal semiconductor film according to claim 1, wherein an area of a magnetic field generated by the electromagnetic induction is wider than an irradiated area by the high energy pulse beam so that only the liquid part is heated with the electromagnetic induction heating.

5. A method for manufacturing a polycrystal semiconductor film comprising the steps of:

irradiating a high energy pulse beam onto a surface of a semiconductor film comprising an amorphous or first polycrystal semiconductor formed on a first surface of a substrate to melt only the semiconductor film; and

solidifying and forming the semiconductor film comprising a polycrystal with a large crystal grain diameter by passing through a solid-liquid coexisting state;

wherein only a liquid part generated by melting the semiconductor film is heated by using a difference in an electric resistance between a solid part and a liquid part in the solid-liquid coexisting state so as to prolong a solidification time until the completion of the solidification of the semiconductor film which has been molten; and

wherein the heating of the liquid part is the electric heating, the heating being carried out by applying a voltage between conductors provided adjacent to the semiconductor film to subject to resistance-heating.

6. The method for manufacturing the polycrystal semiconductor film according to claim 5, wherein an area of electric heating of the semiconductor film is overlapped with an irradiation area by the high energy pulse beam.

7. The method for manufacturing the polycrystal semiconductor film according to claim 5, wherein the voltage is controlled for electric heating in synchronization with the high energy beam which is irradiated to the surface of the semiconductor film so as to correct a lowering of a heating efficiency due to an increase of resistance generated by the change of the ratio of the solid and liquid during the progress of the solidification.

8. A method for manufacturing a polycrystal semiconductor film comprising the steps of:

irradiating a high energy pulse beam to a semiconductor film comprising an amorphous or a first polycrystal semiconductor to melt the semiconductor film, and thereafter solidifying the film to form a polycrystal semiconductor film having an improved crystallinity,

wherein a material having a melting point of 1600° C. or more and a thermal conductivity of 0.01 cal/cm.s.° C. at 1000° C. or less is used as a base film of the semiconductor film, and time up to the complete solidification of the semiconductor film can be prolonged by suppressing the heat dissipation from the molten film of the semiconductor to the substrate.

9. A method for manufacturing a polycrystal semiconductor film comprising the steps of:

irradiating a high energy pulse beam onto a surface of a semiconductor film comprising an amorphous or first polycrystal semiconductor formed on a first surface of a substrate to melt only the semiconductor film; and

solidifying and forming the semiconductor film comprising a polycrystal with a large crystal grain diameter by passing through a solid-liquid coexisting state;

wherein only a liquid part generated by melting the semiconductor film is heated by using a difference in an electric resistance between a solid part and a liquid part in the solid-liquid coexisting state so as to prolong a solidification time until the completion of the solidification of the semiconductor film which has been molten; and

wherein a material having a melting point of 1600° C. or more and a thermal conductivity of 0.01 cal/cm.s.° C. or less is used as a base film of the semiconductor film so as to prolong a solidification time until the complete solidification by suppressing heat dissipation from the molten liquid of the semiconductor film to the substrate.

10. A method for manufacturing a polycrystal semiconductor film comprising the steps of irradiating a high energy

beam onto a semiconductor film comprising an amorphous semiconductor or a polycrystal semiconductor to melt the semiconductor film, and solidifying the semiconductor film via a solid and liquid coexisting state to form the polycrystal semiconductor,

wherein the high energy beam is irradiating to form a standing wave at a predetermined position of the surface of the semiconductor, and to generate a heat density distribution having the same cycle as the standing wave at the predetermined position, thereby the semiconductor film being melted.

11. The method for manufacturing the polycrystal semiconductor film according to claim **10**, wherein the standing wave is formed by irradiating at least two laser beams with incident angle capable of forming the standing wave to the semiconductor film.

12. The method for manufacturing the polycrystal semiconductor film according to claim **10**, wherein the standing wave is formed by irradiating at least one laser beam at a predetermined incident angle and in the polarization state.

13. The method for manufacturing the polycrystal semiconductor film according to claim **10**, wherein a cycle of the heat density distribution is set to 1 to 10 μm.

14. The method for manufacturing the polycrystal semiconductor film according to claim **10**, wherein the method further comprises a step of prolonging a solidification time by using a difference in a electric resistance between the solid and the liquid in the solid and liquid coexisting state to heat only the liquid.

15. The method for manufacturing the polyscrystal semiconductor film according to claim **10**, wherein a material having a melting point of 1600° C. and a thermal conductivity of 0.01 cal/cm.s.° C. is used as a base film of the semiconductor film to suppress heat dissipation from the molten liquid of the semiconductor to the substrate side so as to prolong a solidification time until the complete solidification.

16. The method for manufacturing the polycrystal semiconductor film according to claim **14**, wherein a material having a melting point of 1600° C. and a thermal conductivity of 0.01 cal/cm.s.° C. is used as a base film of the semiconductor film to suppress heat dissipation from the molten liquid of the semiconductor to the substrate side so as to prolong a solidification time until the complete solidification.

17. The method for manufacturing the polycrystal semiconductor film according to claim **11**, wherein a cycle of the heat density distribution is set to 1 to 10 μm.

18. The method for manufacturing the polycrystal semiconductor film according to claim **12**, wherein a cycle of the heat density distribution is set to 1 to 10 **82** μm.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,970,368

DATED : October 19, 1999

INVENTOR(S) : Hideyuki SASAKI ET AL.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 1, line 7, change "polycrysal" to --polycrystal--;

line 20, change "quarz" to --quartz--;

line 30, change "quarz" to --quartz--.

Col. 8, line 28, change "polycrysal" to --polycrystal--.

Signed and Sealed this

Twenty-second Day of May, 2001

Attest:

Nicholas P. Godici

NICHOLAS P. GODICI

Attesting Officer

Acting Director of the United States Patent and Trademark Office

US006056848A

United States Patent [19]

Daviet

[11] Patent Number: 6,056,848

[45] Date of Patent: May 2, 2000

[54] **THIN FILM ELECTROSTATIC SHIELD FOR INDUCTIVE PLASMA PROCESSING**

[75] Inventor: **Jean-François Daviet**, Cran-Gevrier, France

[73] Assignee: **CTP, Inc.**, San Jose, Calif.

[21] Appl. No.: **08/926,873**

[22] Filed: **Sep. 10, 1997**

Related U.S. Application Data

[60] Provisional application No. 60/027,013, Sep. 11, 1996.

[51] **Int. Cl.**[7] **H01L 21/00**

[52] **U.S. Cl.** ..... **156/345**; 118/723 IR; 118/723 I; 216/68; 438/729; 438/730

[58] **Field of Search** ..... 156/345; 118/723 I, 118/723 IR; 216/68; 438/729, 730

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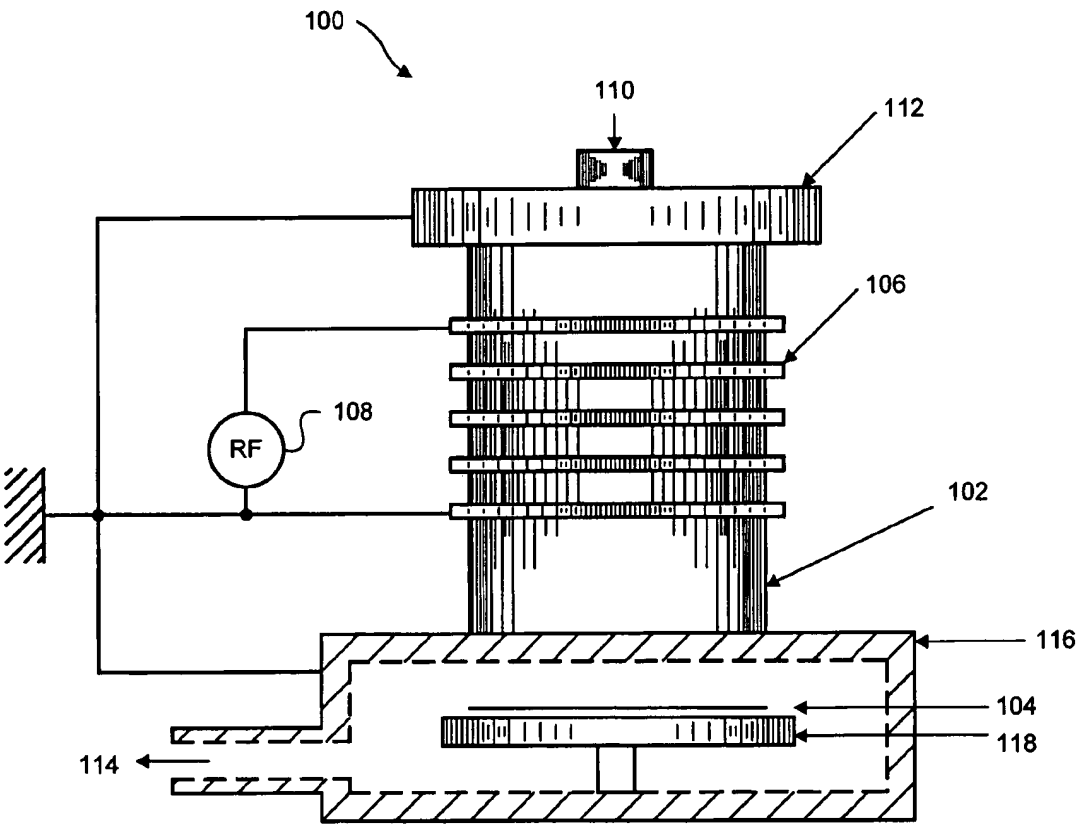
[57] **ABSTRACT**

A plasma reactor and methods for processing semiconductor substrates are described. An induction coil inductively couples power into the reactor to produce a plasma. A thin electrostatic shield is interposed between the induction coil and plasma to reduce capacitive coupling. The shield is electromagnetically thin such that inductive power passes through the shield to sustain the plasma while capacitive coupling is substantially attenuated. Reducing capacitive coupling reduces modulation of the plasma potential relative to the substrate and allows for more controllable processing.

60 Claims, 3 Drawing Sheets



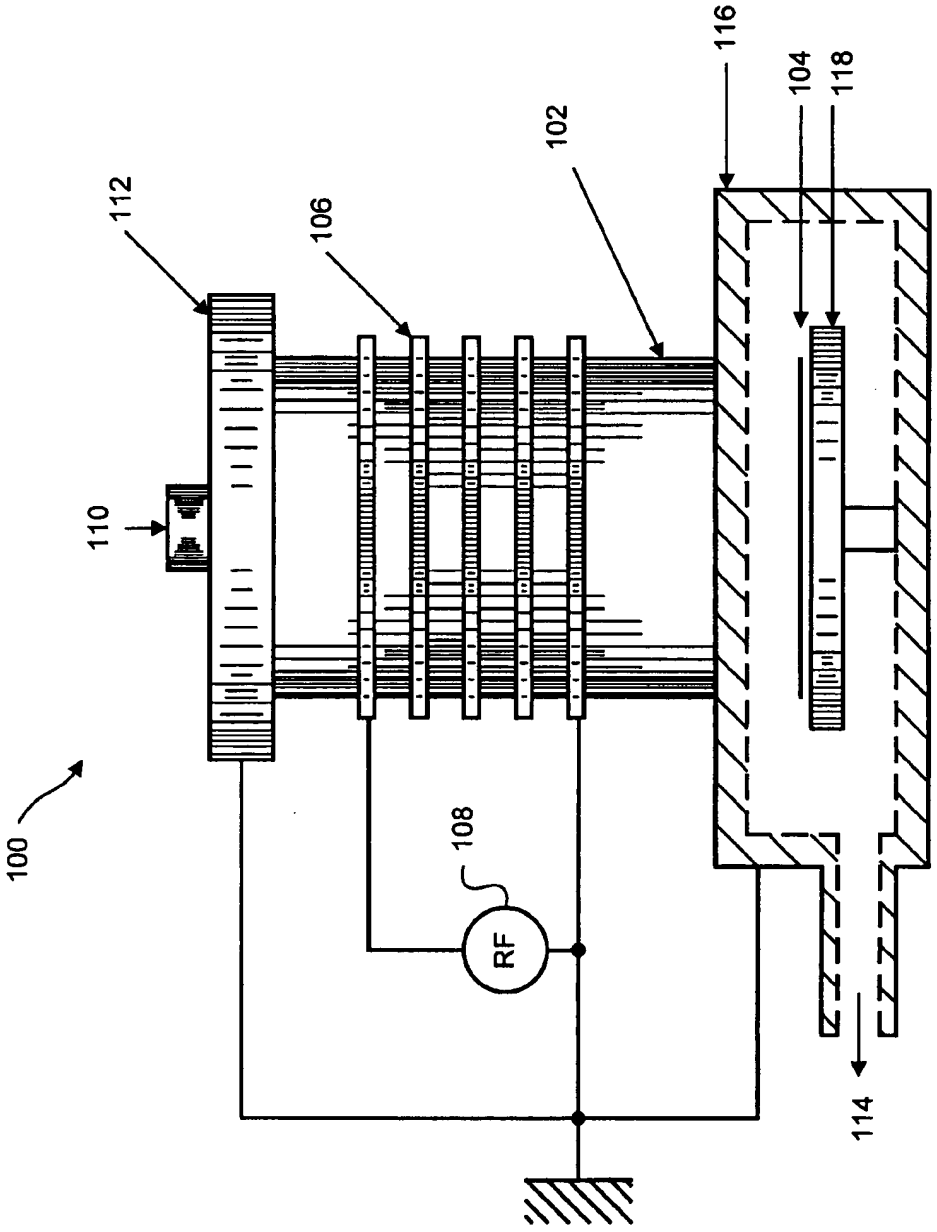


Figure 1

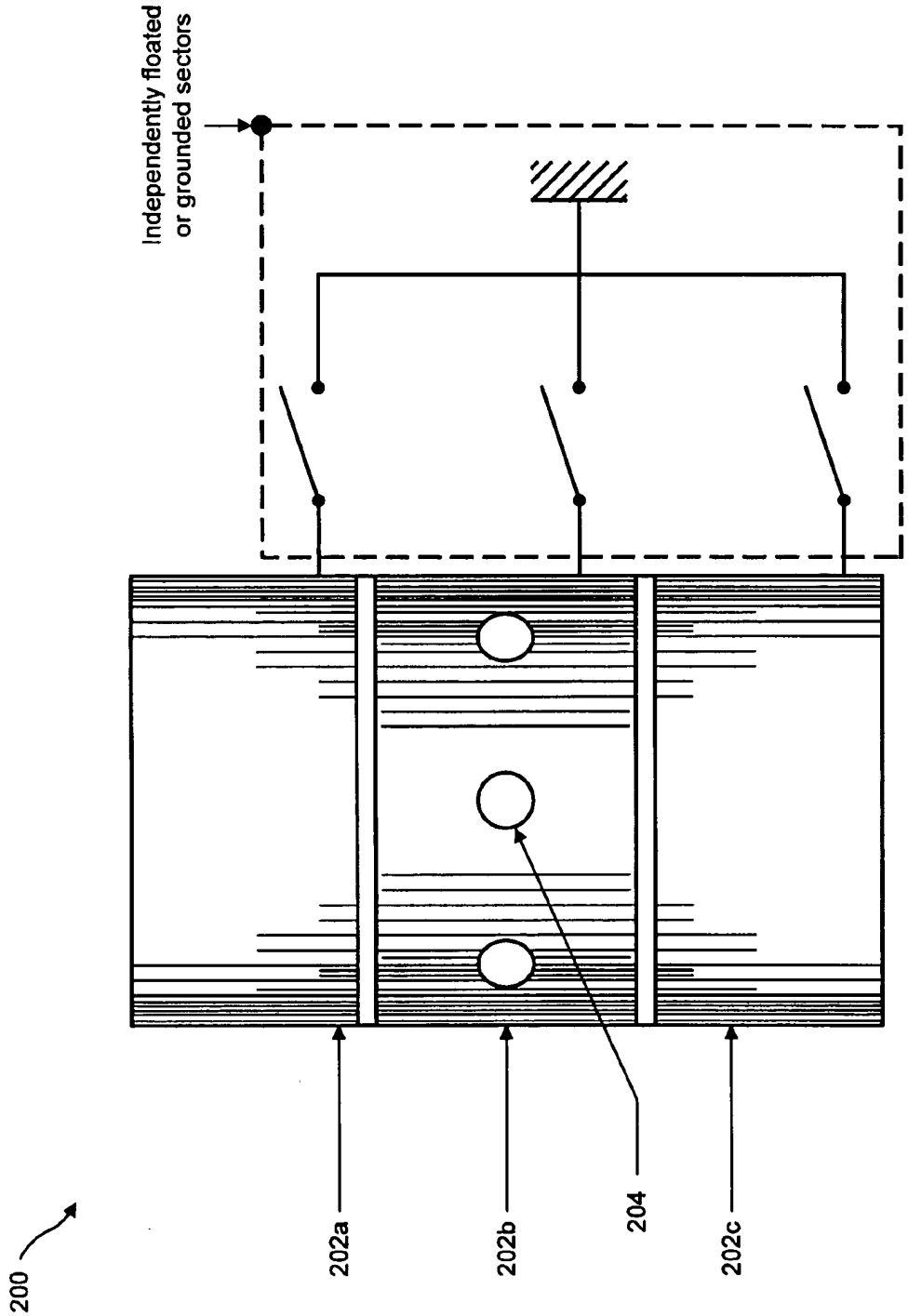

Independently floated
or grounded sectors
200
202a
202b
204
202c

Figure 2

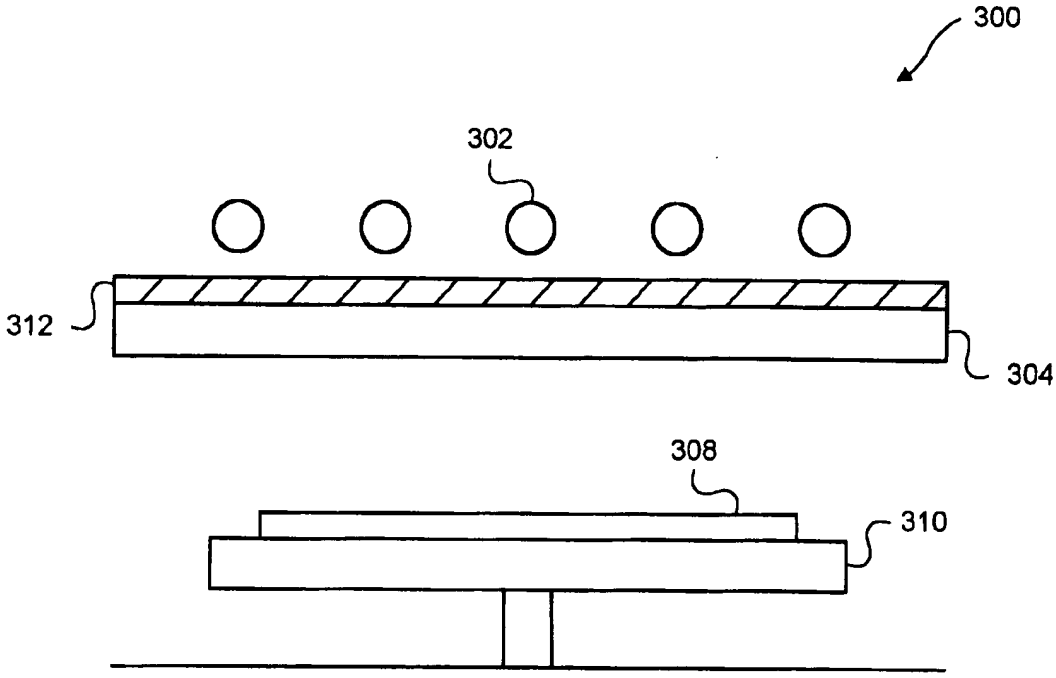


Figure 3A

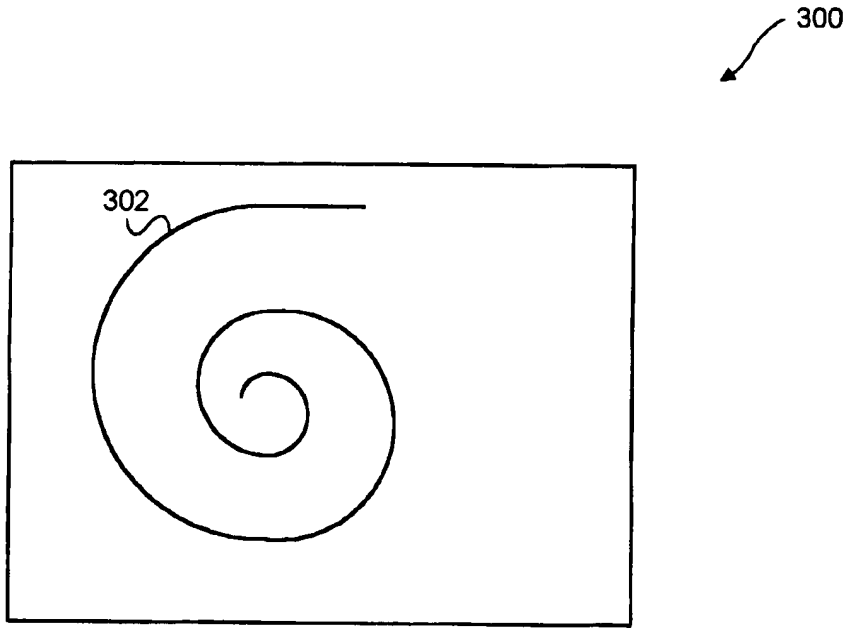


Figure 3B

THIN FILM ELECTROSTATIC SHIELD FOR INDUCTIVE PLASMA PROCESSING

REFERENCE TO RELATED APPLICATION

The present application claims priority from provisional application No. 60/027,013, filed Sep. 11, 1996. Provisional application No. 60/027,013 is hereby incorporated by this reference in its entirety.

BACKGROUND

1. Field of the Invention

The field of the present invention relates in general to plasma reactors and processes typically used to process semiconductor substrates or the like. More particularly, the field of the invention relates to a shielded plasma reactor in which the plasma is generated primarily by inductively coupled power.

2. Background

The era of microelectronics, and more specifically of Very Large Scale Integration, has been built in large part around vacuum processing of semiconductors to obtain Integrated Circuits. One of the contributors in this field of vacuum processing, which enabled the development and success of today's semiconductor industry, is undoubtedly the outstanding parallel development of plasma tools and of related processing techniques. The plasma-based equipment market is a multi-billion dollar annual business, be it for thin film deposition, etching or even ion implantation.

The history of plasma etching is relatively short, starting only around twenty years ago. The first commercially available equipment featured a basic diode-like configuration. The plasma was generated in a vacuum chamber between two flat electrodes. One of the electrodes was typically used as a wafer susceptor, and was also usually connected to a high-frequency power supply. The other electrode was typically grounded, although in some configurations the second electrode was connected to a high frequency power supply instead of or in addition to the first electrode. This configuration was very successful at the time, but important technological limitations started to become evident in the early eighties. As integrated circuit geometry continued to shrink dramatically, the semiconductor industry sought to develop plasma equipment capable of producing dense plasmas with low energy ions. A dense plasma is important in order to achieve a high rate of processing, while low energy ions are important to avoid damaging small integrated circuit features which are susceptible to damage from bombardment of high energy ions. In order to produce a high density, low ion energy plasma, it is desirable to de-couple the control of plasma density from the control of ion energy in a plasma.

The first serious generation of decoupled, or advanced, plasma sources that appeared in the eighties relied on a microwave power source and featured a special magnet arrangement (technology known as Electronic Cyclotron Resonance, or ECR) capable of delivering a high plasma density without high energy ion bombardment of the semiconductor wafer. The usefulness of conventional ECR to address the evolving needs of the semiconductor industry is limited, however, mainly because of the complexity and very limited operating pressure range of conventional ECR.

A more promising approach has more recently emerged based upon the conventional *Inductively Coupled Plasma*, or ICP, which was originally invented at the end of the 19th century. Modern ICP sources, which have been improved and adapted for use in semiconductor processing, appear to provide a technology with the potential to meet the needs of the semiconductor industry well into the next decade. While ICP and ECR both provide high density, low ion energy plasmas, ICP allows a drastically wider pressure range to be used for processing. The pressure range for typical ICP sources ranges from about 0.5 mtorr to about 1 torr, whereas typical ECR sources are limited to an operating range of about 0.5 mtorr to about 5 mtorr. Consequently, ICP is suitable for a very wide range of applications that intrinsically require very different process pressures—from low pressure, fine pattern anisotropic etching to high pressure, isotropic etching.

Nevertheless, some conventional ICP sources suffer from a disadvantage in that they are prone to generate a significant amount of energetic ions. This is caused by the fact that the induction coil used to inductively couple energy into the plasma also causes some capacitive coupling of electromagnetic energy between the metal coil and the plasma (a phenomenon called parasitic capacitive coupling of the ICP inductor). In a typical ICP reactor, an induction coil surrounds a plasma production chamber below which a semiconductor substrate is placed for processing. Radio frequency power is applied to the induction coil and thereby inductively coupled into the plasma production chamber. The inductively coupled power accelerates ions circumferentially in the plasma substantially parallel to the semiconductor substrate. While inductively coupled power from the induction coil tends to accelerate ions in a plane parallel to the semiconductor substrate, the parasitic capacitive coupling tends to accelerate ions radially outward from the plasma which causes high energy ions to bombard the semiconductor substrate below the plasma. This problem is described in detail in U.S. Pat. No. 5,534,231 the disclosure of which is hereby incorporated herein by reference in its entirety.

This parasitic capacitive coupling can be substantially blocked by using a split electrostatic shield, also known as a split Faraday shield, positioned between the induction coil and the dielectric plasma chamber wall. The shield substantially blocks capacitive coupling while allowing inductive coupling of power into the plasma. Conventional split electrostatic shields typically comprise metal plates or a metal cylinder forming longitudinal slits transverse to the induction coil. The metal body of the shield blocks capacitive coupling, while the slits allow inductively coupled power to penetrate the shield. The slits prevent circumferential current loops from forming in the shield which would otherwise substantially prevent the penetration of the inductive electric field. Such electrostatically shielded ICP reactors are described in U.S. Pat. No. 4,918,031, U.S. Pat. No. 5,234,529 and U.S. Pat. No. 5,534,231, each of which is hereby incorporated herein by reference in its entirety. The excellent performance of such electrostatically shielded ICP sources demonstrates the promising potential of this technology for use in future semiconductor plasma processing equipment. Nevertheless, conventional split electrostatic shields are not ideal for all plasma processing. The slits allow some capacitive coupling through the slits which may in turn cause non-uniform power deposition in the plasma. In addition, conventional electrostatic shields typically comprise relatively complex, bulky and expensive solid-metal structures that must be fitted and supported around the outside of the dielectric ICP chamber wall.

What is needed is an electrostatic shield for ICP semiconductor processing reactors which provides more uniform and continuous shielding around the plasma. What is also need is an electrostatic shield that provides improved shield-

ing of capacitive electric fields while allowing virtually unimpeded penetration of inductive electric fields. Preferably such an improved shield will be inexpensive and easy to manufacture and deploy.

SUMMARY OF THE INVENTION

One aspect of the present invention provides a thin film electrostatic shield for an inductively coupled plasma source for use in plasma processing. The thin film electrostatic shield provides a thin layer of conductive material between a source of inductively coupled power and a plasma. The conductive material is capable of blocking a desired amount of parasitic capacitive coupling from the power source or other source of capacitive power. In particular embodiments, a continuous thin film electrostatic shield (without slits or gaps) may be used between the source of capacitive power and the plasma, providing virtually complete capacitive shielding of the plasma. In other embodiments, the shield may contain slits or gaps to allow a desired amount of capacitive coupling. The slits or gaps do not have to be arranged transverse to the induction electric field as with conventional split electrostatic shields. Rather gaps can be arranged in any variety of patterns. For instance, small holes or gaps may be uniformly distributed around the shield to allow more uniform capacitive power deposition in the plasma.

The electrostatic shield is preferably sufficiently thin, so as to allow the inductive electric field to penetrate the shield and sustain the plasma. Unlike conventional split electrostatic shields, a longitudinal slit in the shield is not required to prevent circumferential currents in the shield and to allow power to be inductively coupled into the plasma. Rather, the fact that the shield is very thin allows power to be inductively coupled into the plasma through the shield with very little power loss. The thickness of the shield may be configured to allow a desired amount of inductively coupled power to penetrate the shield, although typically the shield is sufficiently thin such that substantially all of the inductive power penetrates the shield.

It is an advantage of these and other aspects of the present invention that capacitive power may be almost completely blocked, while inductive power is allowed to penetrate the shield virtually unimpeded. In particular, a continuous shield may be used in various embodiments without substantially blocking inductively coupled power as would be the case with a conventional continuous thick metal shield. It is a further advantage that gaps in any variety of patterns may be provided in the shield to allow a desired amount of capacitive coupling. The gaps need not be arranged in any specific relation to the source of inductively coupled power. In addition, the thickness of the shield may be selected to allow a desired amount of inductive power to penetrate the shield.

Another aspect of the present invention provides for a thin electrostatic shield that is deposited on, or forms a portion of, a plasma chamber wall. In particular embodiments, a thin layer of conductive material may be deposited directly onto a non-conductive chamber wall comprising quartz or other material substantially inert to the plasma processing environment.

It is an advantage of these and other aspects of the present invention that electrostatic shielding may be provided without a separate, bulky and expensive metal split electrostatic shield. Rather, the electrostatic shielding may be provided directly as part of the chamber wall or induction coil without the requirement of a separate stand-alone structure external to the chamber wall.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention will become more apparent to those skilled in the art from the following detailed description in conjunction with the appended drawings in which:

FIG. **1** is a side, partially cross-sectional view of an electrostatically shielded ICP reactor according to a first embodiment of the present invention;

FIG. **2** is a side view of an electrostatic shield according to a second embodiment of the present invention;

FIG. **3A** is a side, cross-sectional view of an electrostatically shielded ICP reactor according to a third embodiment of the present invention; and

FIG. **3B** is a top view of an electrostatically shielded ICP reactor according to the third embodiment of the present invention.

DESCRIPTION

One aspect of the present invention provides a thin electrostatic shield for an inductively coupled plasma source for use in plasma processing. The following description is presented to enable any person skilled in the art to make and use the invention. Descriptions of specific designs are provided only as examples. Various modifications to the exemplary embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

In the embodiments described herein, a variety of known components of inductively coupled plasma reactors and methods for processing semiconductors and other substrates may be used in conjunction with aspects of the present invention including without limitation radio frequency power sources, radio frequency powered susceptors or electromagnetically isolated susceptors, gas supply systems, gas exhaust systems, wafer transport and handling mechanisms, induction coils, plasma production chambers, processing chambers, anisotropic and isotropic etch processing, pulsed power processing as well as components and methods that may be developed in the future. Detailed descriptions of many such components and processes which may be used in conjunction with the present invention are described in U.S. Pat. No. 4,918,031, U.S. Pat. No. 5,234,529, U.S. Pat. No. 5,534,231 and International Patent Application published under the PCT as International Publication No. WO96-15545, each of which is hereby incorporated herein by reference in its entirety. In particular, a thin electrostatic shield according to the present invention may be used in place of a conventional shield in the helical resonators and other ICP reactors described in the above-referenced patents and published application.

Aspects of the present invention provide an improved electrostatic shield specifically designed for superior performance for plasma processing of semiconductors, flat panel displays or other substrates. The features of an ideal, complete electrostatic shield for inductively coupled processing include: (i) perfect opacity to electrostatic fields generated by the inductor, and (ii) perfect transparency to the inductive electromagnetic field. It has been found that a continuous, electromagnetically thin layer of conductive material between the inductor and the plasma can be used to provide virtually ideal electrostatic shielding. Note that this electro-

magnetically thin layer of conductive material can be physically implemented in numerous ways, as long as it is set between the inductor and the plasma.

The most straightforward way is to coat the dielectric chamber with such a material. Another way is to wrap the chamber with a dielectric film (such as Hylar or Kapton), on which the desired film has been previously deposited. Just as effective would be any structure allowing the direct wrapping of the inductor itself (instead of the dielectric chamber): one could for example provide a coaxial inductor where the core would be made of solid metal, and where the outer metal sheath (separated from the core by a dielectric sheath) would be so thin as to meet the criteria for being a thin film electrostatic shield.

An electromagnetic wave with a frequency f (e.g., an inductive field at a frequency of 13.56 MHz) is indeed absorbed exponentially with the penetration depth in a conductive material, with a characteristic distance (or skin depth) δ:

$$\delta (\rho/f)^{1/2},$$

ρ being the electrical resistivity of the material. An electromagnetically thin layer can be defined, for a given electromagnetic frequency, as a film of material whose thickness is less than three times the skin depth of the material for the given frequency.

An electrostatic shield using an electromagnetically thin layer of conductive material is substantially thinner than typical conventional split electrostatic shields used in semiconductor processing. For instance, a split electrostatic shield described in International Patent Application published under the PCT as International Publication No. WO96-15545 has a width of approximately 115 thousandth of an inch (i.e., 0.002875 meters) in the section of the shield adjacent to the induction coil (which contains the slots that allow penetration of inductively coupled power). In a thin electrostatic shield according to embodiments of the present invention, the portion of the shield adjacent to the induction coil may be more than ten times thinner (e.g., less than about 250 microns) and may be in the range of, for example, from about 0.05 to about 5 microns in width.

Considering for example aluminum, the skin depth at 13.56 MHz is about 20 μm. A very straightforward calculation using this skin depth shows that if we coat the dielectric chamber wall of a typical ICP reactor with a layer of aluminum with a thickness of 0.1 μm, the inductive energy loss in this layer is expected to be less than about 0.5%.

The conductivity of the aluminum layer is sufficient, however, to remain equipotential even when parasitically coupled to the inductor. When the aluminum layer is further connected to ground (or to a solid-metal chamber body), the plasma in the enclosure of the process chamber is virtually perfectly electrostatically shielded.

Beyond the major technological advantages inherently provided by a Thin Film Electrostatic Shield (or TFES), namely a virtually perfect electrostatic shielding with almost no inductive power loss, the intrinsic simplicity of the TFES also has a tremendous industrial benefit, when compared to its complex, bulky and expensive solid-metal counterpart.

The basic concept of a thin electrostatic shield may be applied in any variety of configurations to support different types of processing. Some embodiments may, for instance: (i) provide limited open areas in the shield to ease the plasma ignition (especially for low power operation); (ii) provide a shield divided into several electrically independent sectors that can be independently grounded, or biased; (iii) provide mechanisms for adjusting the level of capacitive coupling of some sectors during the process (for instance by providing an elevational or rotational actuator for lifting portions of the shield or moving them apart to provide gaps that allow conductive coupling); or (iv) provide different thickness in different areas, e.g. for the purpose of controlling power distribution throughout the chamber. It should also be noted that embodiments of a thin electrostatic shield may be useful for fields other than plasma processing. For thermal processing under vacuum (frequency typically <100 kHz), for example, a thin electrostatic shield may be used to prevent the ignition of an undesired plasma.

FIG. **1** is a side, partially cross-sectional view of an exemplary electrostatically shielded ICP reactor, generally indicated at **100**, according to a first embodiment of the present invention. In the first embodiment, a dielectric vessel **102** forms a plasma chamber within which a plasma is produced for processing a semiconductor wafer **104** or other substrate. The dielectric vessel **102** in the first embodiment comprises quartz or alumina on which a thin electrostatic shield is deposited. An inductor **106** is provided adjacent to the plasma chamber to inductively couple power into the plasma in the plasma chamber. In the first embodiment, the inductor **106** comprises a helical coil surrounding the dielectric vessel **102**. Of course, other inductors may be used in other embodiments, including without limitation, helical resonator coils, spiral coils in a flat plane or cone next or above the plasma chamber, or other inductors for inductively coupling power into the plasma chamber. A power source **108** provides radio frequency power to the inductor at a desired frequency. In the first embodiment, frequencies in the range of from about 0.1 MHz to about 40.68 MHz (or any range subsumed therein) might be used depending upon the desired processing, with a frequency of 13.56 MHz typically being used. In the first embodiment, gas is provided from a conventional gas source and is injected into the plasma chamber through a gas inlet **110** formed in the top of the chamber **112**. Gas is exhausted from the reactor through a gas exhaust **114** which is coupled to a pump or other conventional exhaust system. Below the plasma chamber is a processing chamber **116** in which is contained a wafer **104** for processing. A susceptor **118** provides a support for the wafer. The susceptor may be isolated from ground or may be biased with RF power or other electric or magnetic field to attract or repel ions in a controllable manner.

In the first embodiment, RF power is inductively coupled into the gas in the plasma chamber to form a plasma. The plasma contains plasma products including ions, dissociated atoms and excited molecules. The wafer may be exposed to selected plasma products for processing. For instance, ions may be accelerated toward the wafer for anisotropic etching. Alternatively, ions may not be accelerated toward the wafer (and may in fact be repelled or filtered) and dissociated atoms may be used for isotropic ashing. Any variety of other processes may be performed as well.

In the first embodiment, a thin film electrostatic shield is deposited on the dielectric vessel to shield against parasitic capacitance from the inductor **106**. In the first embodiment, the shield comprises a thin layer of material with a conductivity sufficient to substantially block capacitive coupling through the material when the shield is grounded or held at some desired potential. In the first embodiment, a low impedance path for the given power frequency is provided between the shield and ground. In particular, the shield is electrically connected to the chamber top and processing

chamber walls which are grounded. The shield may also be grounded in additional locations to prevent voltage differences from appearing along the body of the shield. In the first embodiment, the conductivity of the material used to form the shield is preferably less than about 1 Ω.cm. An exemplary shield for the first embodiment comprises a thin film of aluminum or titanium nitride (which provides better mechanical resistance) with a thickness in the range of about one hundredth of a micron to about 60 microns (or any range subsumed therein) and a preferred thickness in the range of about 0.1 micron to about 5 microns. The aluminum film may be deposited directly on the external dielectric vessel wall using conventional deposition techniques. As described above, this shield substantially blocks capacitive coupling of the inductor to the plasma, while allowing inductive power to penetrate the shield and sustain the plasma in the plasma chamber.

FIG. **2** is a side view of an electrostatic shield, generally indicated at **200**, according to a second embodiment of the present invention. As in the first embodiment, the electrostatic shield may comprise a thin film of around 0.1–5 μm of aluminum or titanium nitride (better mechanical resistance) deposited on a dielectric vessel. In the second embodiment, however, the shield is divided into three electrically independent sectors **202***a, b* and *c*, each of substantially the same height. Each sector may be independently grounded or left electrically floating which provides more control over generating and sustaining the plasma and in turn more process flexibility. The second embodiment also contains 4–6 small, circular unshielded areas **204** formed in the thin film coating (diameter=10 mm) evenly distributed at around ⅔ the height of vessel. Such unshielded gaps may be used to allow a controlled amount of capacitive coupling which makes it easier to ignite a plasma at low power.

Of course any variety of configurations may be used to control plasma characteristics. Capacitive coupling in different areas of the plasma may be controlled by providing either shielding or unshielded gaps in desired locations. Inductive coupling may be controlled by adjusting the power source or by varying the thickness of the shield in desired locations such that the shield absorbs some amount of inductive power. In some embodiments, if power is absorbed by the shield, the shield may have to be cooled. Water cooling or other conventional cooling mechanisms may be used for this purpose.

FIG. **3**A is a side, cross-sectional view, and FIG. **3**B is a top view, of an electrostatically shielded ICP reactor, generally indicated at **300**, according to a third embodiment of the present invention. In the third embodiment, the inductor **302** is in a flat or "pancake" configuration. The inductor is adjacent to a top dielectric wall **304** of the reactor and forms a spiral as shown in FIG. **3**B (although other configurations may be used to inductively couple power into such a flat reactor configuration as well). The inductor inductively couples power into a plasma processing chamber **306** to form a plasma. A wafer **308** or other substrate is supported in the plasma processing chamber on a susceptor **310** for processing. A thin electrostatic shield **312** is provided between the inductor and the plasma to block parasitic capacitance as in the embodiments described above. In the third embodiment, a thin layer of aluminum or titanium nitride with a thickness of from about 0.1 micron to about 5 microns may be deposited directly onto the external surface of the top dielectric wall of the reactor.

It will be readily apparent to those of ordinary skill in the art that the above techniques may be applied in any variety of inductively coupled processing systems and methods.

While this invention has been described and illustrated with reference to particular embodiments, the scope of the present invention is not limited to the disclosed embodiments but, on the contrary, is intended to cover numerous other modifications and equivalent arrangements which are included within the spirit and scope of the following claims.

What is claimed is:

1. An apparatus comprising:

a chamber wall forming a process chamber;

an electrostatic shield adjacent to at least a portion of the process chamber;

the electrostatic shield comprising a highly conductive material such that electrostatic fields are substantially prevented from penetrating through the electrostatic shield into the process chamber; and

at least a portion of the electrostatic shield being sufficiently thin such that inductive electromagnetic fields penetrate through the electrostatic shield into the process chamber at a desired level for processing.

2. The apparatus of claim **1** wherein the chamber wall comprises an electrically resistive material and the electrostatic shield substantially covers the electrically resistive material of the chamber walls.

3. An apparatus comprising:

a chamber wall forming a process chamber;

the chamber wall comprising an electrically resistive material having a resistivity greater than about 1 Ω cm;

an electrostatic shield adjacent to at least a portion of the process chamber;

the electrostatic shield comprising a highly conductive material having a resistivity of less than about 1 Ω cm such that electrostatic fields are substantially prevented from penetrating through the electrostatic shield into the process chamber; and

the electrostatic shield being sufficiently thin such that inductive electromagnetic fields penetrate through the electrostatic shield into the process chamber at a desired level for processing,

wherein the electrostatic shield comprises a plurality of regions each having a different thickness of the conductive material.

4. An apparatus comprising:

a chamber wall forming a process chamber;

the chamber wall comprising an electrically resistive material having a resistivity greater than about 1 Ω cm;

an electrostatic shield adjacent to at least a portion of the process chamber, the electrostatic shield comprising a highly conductive material having a resistivity of less than about 1 Ω cm such that electrostatic fields are substantially prevented from penetrating through the electrostatic shield into the process chamber; and

the electrostatic shield being sufficiently thin such that inductive electromagnetic fields penetrate through the electrostatic shield into the process chamber at a desired level for processing,

wherein the electrostatic shield forms a plurality of substantially non-conductive gaps such that the electrostatic shield includes a plurality of conductive sectors electrically isolated from one another.

5. The apparatus according to claim **3** wherein at least one of the conductive sectors is electrically coupled to a ground potential.

6. The apparatus according to claim **3** wherein at least one of the conductive sectors is electrically coupled to a power supply.

7. The apparatus according to claim 1 further comprising an inductor adjacent to the process chamber for inductively coupling power into the process chamber.

8. The apparatus according to claim 7, wherein the inductor is a loop-like coil.

9. The apparatus according to claim 7, wherein the inductor is a spiral-like coil.

10. The apparatus according to claim 7, wherein the inductor is a solenoid-like coil.

11. The apparatus according to claim 7, wherein the inductor is a helical resonator.

12. An apparatus according to claim 7, further comprising a gas inlet for providing gases into the process chamber, wherein the inductor inductively couples power into the process chamber to sustain a plasma in the process chamber.

13. A plasma reactor for processing a semiconductor substrate comprising:

a chamber wall forming a plasma chamber within which a plasma is produced;

the plasma including at least one plasma product for processing the substrate;

a source of radio frequency power;

an inductor adjacent to the plasma chamber and coupled to the source of radio frequency power to inductively couple power into the plasma chamber;

a gas inlet for providing gas into the plasma chamber;

a gas exhaust for exhausting gas from the plasma chamber;

an electrostatic shield positioned between at least a portion of the inductor and at least a portion of the plasma such that the electrostatic shield reduces capacitive coupling from the inductor to the plasma relative to a level of capacitive coupling that would be present in the absence of the thin electrostatic shield;

wherein at least a portion of the electrostatic shield has a thickness less than about 250 microns such that inductively coupled power from the inductor is coupled through the electrostatic shield to sustain the plasma; and

wherein the substrate is positioned such that the substrate is exposed to the at least one plasma product for processing.

14. The plasma reactor according to claim 13 wherein the electrostatic shield comprises a thin film having a thickness of less than about 100 microns.

15. The plasma reactor according to claim 13 wherein the electrostatic shield comprises a thin film having a thickness of less than about 5 microns.

16. The plasma reactor according to claim 13 wherein the electrostatic shield comprises a conductive material.

17. The plasma reactor according to claim 13 wherein the electrostatic shield comprises a material having a resistivity of less than about 1 Ω cm.

18. The plasma reactor according to claim 13 wherein the electrostatic shield comprises a material selected from the group consisting of aluminum and titanium nitride.

19. The plasma reactor according to claim 13 wherein the electrostatic shield comprises a thin film having a thickness less than three times the skin depth of the thin film for a given frequency of the source of radio frequency power.

20. A plasma reactor for processing a semiconductor substrate comprising:

a non-conductive chamber wall forming a plasma chamber within which a plasma is produced;

the plasma including at least one plasma product for processing the substrate;

a source of radio frequency power;

an inductor adjacent to the plasma chamber and coupled to the source of radio frequency power to inductively couple power into the plasma chamber;

a gas inlet for providing gas into the plasma chamber;

a gas exhaust for exhausting gas from the plasma chamber;

a thin electrostatic shield positioned between at least a portion of the inductor and at least a portion of the plasma chamber such that the thin electrostatic shield reduces capacitive coupling from the inductor to the plasma relative to a level of capacitive coupling that would be present in the absence of the thin electrostatic shield;

wherein the thin electrostatic shield is sufficiently thin such that inductively coupled power from the inductor is coupled through the thin electrostatic shield to sustain the plasma; and

wherein the substrate is positioned such that the substrate is exposed to the at least one plasma product for processing,

wherein the electrostatic shield is deposited on at least a portion of the inductor.

21. The plasma reactor according to claim 13 wherein the thin electrostatic shield is deposited on at least a portion of the chamber wall.

22. The apparatus of claim 1 wherein the electrostatic shield comprises metal.

23. The apparatus of claim 1 wherein the electrostatic shield comprises titanium nitride.

24. The apparatus of claim 1 wherein the electrostatic shield comprises a thin film.

25. The apparatus of claim 1 wherein:

the inductor includes a conductive core; and

the electrostatic shield comprises a thin film deposited around at least a portion of the inductor and is isolated from the conductive core.

26. The apparatus of claim 1 wherein the electrostatic shield comprises a thin film deposited on the chamber wall.

27. The apparatus of claim 1 wherein the electrostatic shield has a thickness of less than about 250 microns.

28. The apparatus of claim 1 wherein the electrostatic shield has a thickness of less than about 5 microns.

29. The apparatus of claim 1 wherein:

the inductor generates an inductive electric field;

the electrostatic shield is configured such that there is a continuous path along the shield in the direction of the inductive electric field; and

a portion of the shield along the continuous path is sufficiently thin to prevent a countervailing current from being formed which would substantially reduce inductive coupling from the inductor to the plasma.

30. The apparatus of claim 1 wherein the electrostatic shield provides a continuous shield body along the shielded portion of the process chamber.

31. The apparatus of claim 30 wherein substantially the entire region of the process chamber adjacent to the inductor is shielded.

32. The apparatus of claim 1 wherein the thin electrostatic shield comprises a thin film having a thickness less than three times the skin depth of the thin film for a given frequency of the source of radio frequency power.

33. The plasma reactor of claim 32 wherein the frequency is 13.56 MHz.

34. The plasma reactor of claim 13 wherein the electrostatic shield comprises a material which would substantially block inductive coupling at thicknesses greater than 250 microns.

35. The plasma reactor of claim 13 wherein:

the inductor generates an inductive electric field;

the electrostatic shield is configured such that there is a continuous path along the shield in the direction of the inductive electric field; and

a portion of the shield along the continuous path is sufficiently thin to prevent a countervailing current from being formed which would substantially reduce inductive coupling from the inductor to the plasma.

36. The plasma reactor of claim 13 wherein the electrostatic shield provides a continuous shield body along the shielded portion of the process chamber.

37. The plasma reactor of claim 36 wherein substantially the entire region of the process chamber adjacent to the inductor is shielded.

38. The plasma reactor of claim 14 wherein the electrostatic shield comprises a highly conductive material.

39. The plasma reactor according to claim 19 wherein the frequency is 13.56 MHz.

40. A method of processing a semiconductor substrate in a plasma reactor comprising:

supplying gas to a reaction chamber;

shielding the gas in the reaction chamber with an electrostatic shield, the electrostatic shield comprising a highly conductive material and having at least a portion that is sufficiently thin to allow the passage of inductively coupled power through the electrostatic shield into the gas in the reaction chamber;

inductively coupling power into the gas in the reaction chamber through said electrostatic shield;

forming at least one plasma product for processing said substrate; and

exposing said substrate to said at least one plasma product.

41. The method of claim 40 further comprising:

generating an inductive electric field;

wherein the electrostatic shield is configured such that there is a continuous path along the shield in the direction of the inductive electric field; and

a portion of the shield along the continuous path is sufficiently thin to prevent a countervailing current from being formed which would substantially reduce inductive coupling from the inductor to the plasma.

42. The method of claim 40 wherein the electrostatic shield comprises aluminum.

43. The method of claim 40 wherein the electrostatic shield comprises titanium nitride.

44. The method of claim 40 wherein the electrostatic shield comprises a thin film.

45. The method of claim 40 wherein the electrostatic shield comprises a thin film deposited on an inductor.

46. The method of claim 40 wherein the electrostatic shield comprises a thin film deposited on the reactor chamber.

47. The method of claim 40 wherein the electrostatic shield has a thickness of less than about 250 microns.

48. The method of claim 40 wherein the electrostatic shield has a thickness of less than about 100 microns.

49. The method of claim 40 wherein the electrostatic shield has a thickness of less than about 5 microns.

50. A method of processing a semiconductor substrate in a plasma reactor comprising the steps of:

supplying gas to a reaction chamber;

shielding the gas in the reaction chamber with an electrostatic shield, the electrostatic shield having at least a portion with a thickness of less than about 250 microns to allow the passage of inductively coupled power through the electrostatic shield into the gas in the reaction chamber;

inductively coupling power into the gas in the reaction chamber through said electrostatic shield;

forming at least one plasma product for processing said substrate; and

exposing said substrate to said at least one plasma product.

51. The method of claim 50 further comprising:

generating an inductive electric field;

wherein the electrostatic shield is configured such that there is a continuous path along the shield in the direction of the inductive electric field; and

a portion of the shield along the continuous path is sufficiently thin to prevent a countervailing current from being formed which would substantially reduce inductive coupling from the inductor to the plasma.

52. The method of claim 50 wherein the electrostatic shield comprises a highly conductive material.

53. The method of claim 50 wherein the electrostatic shield comprises a material which would substantially block inductive coupling at thicknesses greater than 250 microns.

54. The method of claim 50 wherein the electrostatic shield comprises aluminum.

55. The method of claim 50 wherein the electrostatic shield comprises titanium nitride.

56. The method of claim 50 wherein the electrostatic shield comprises a thin film.

57. The method of claim 50 wherein the electrostatic shield comprises a thin film deposited on an inductor.

58. The method of claim 50 wherein the electrostatic shield comprises a thin film deposited on the reactor chamber.

59. The method of claim 50 wherein the electrostatic shield has a thickness of less than about 100 microns.

60. The method of claim 50 wherein the electrostatic shield has a thickness of less than about 5 microns.

* * * * *

US005578521A

United States Patent [19]

Suzuki et al.

[11] Patent Number: 5,578,521

[45] Date of Patent: Nov. 26, 1996

[54] **SEMICONDUCTOR DEVICE WITH VAPORPHASE GROWN EPITAXIAL**

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[73] Assignee: **Nippondenso Co., Ltd.**, Kariya, Japan

[21] Appl. No.: **432,637**

[22] Filed: **May 3, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 845,812, Mar. 9, 1992, abandoned, which is a continuation of Ser. No. 420,721, Oct. 11, 1989, abandoned, which is a continuation of Ser. No. 123,549, Nov. 20, 1987, abandoned.

[30] **Foreign Application Priority Data**

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Nov. 26, 1986 [JP] Japan 61/281252

[51] **Int. Cl.**[6] **C30B 25/14**

[52] **U.S. Cl.** **437/112**; 437/81; 437/107; 437/116; 437/132; 117/94; 117/95; 117/954

[58] **Field of Search** ..... 117/94, 95, 954; 437/81, 82, 107, 111, 112, 116, 132, 946, 973; 148/DIG. 25, DIG. 51, DIG. 65, DIG. 72, DIG. 91, DIG. 110, DIG. 119, DIG. 148, DIG. 169

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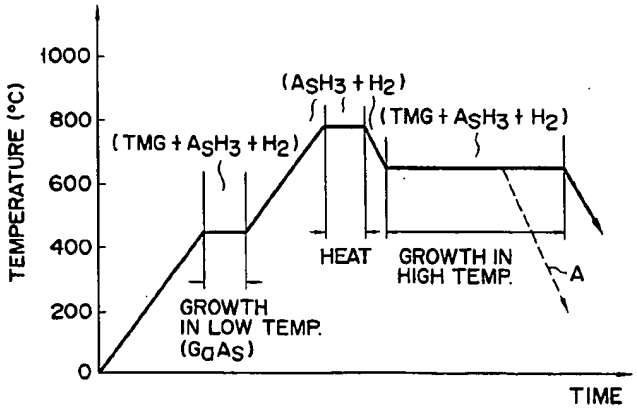
Primary Examiner—Robert Kunemund
Attorney, Agent, or Firm—Cushman Darby & Cushman, L.L.P.

[57] **ABSTRACT**

A silicon semiconductor substrate, on which an epitaxial layer is to be formed, is set in a reaction vessel having a heating mechanism, and a gas containing TMG and AsH_3 is introduced into the reaction vessel with the substrate heated to 450° C., thus forming, on the substrate, a low-temperature growth layer of amorphous or polycrystalline GaAs as a semiconductor substance having a different lattice constant from that of the substrate. Then, with the TMG removed from the introduced gas, the temperature of the semiconductor substrate is increased to 750° C., to cause coagulation of atoms of the low-temperature growth layer, with a thermal treatment also being performed at this high temperature, to cause growth of island-like single crystal cores. Further, a high temperature growth process is conducted in a material gas atmosphere containing TMG, whereby a GaAs film is epitaxially grown on the semiconductor substrate surface.

12 Claims, 6 Drawing Sheets



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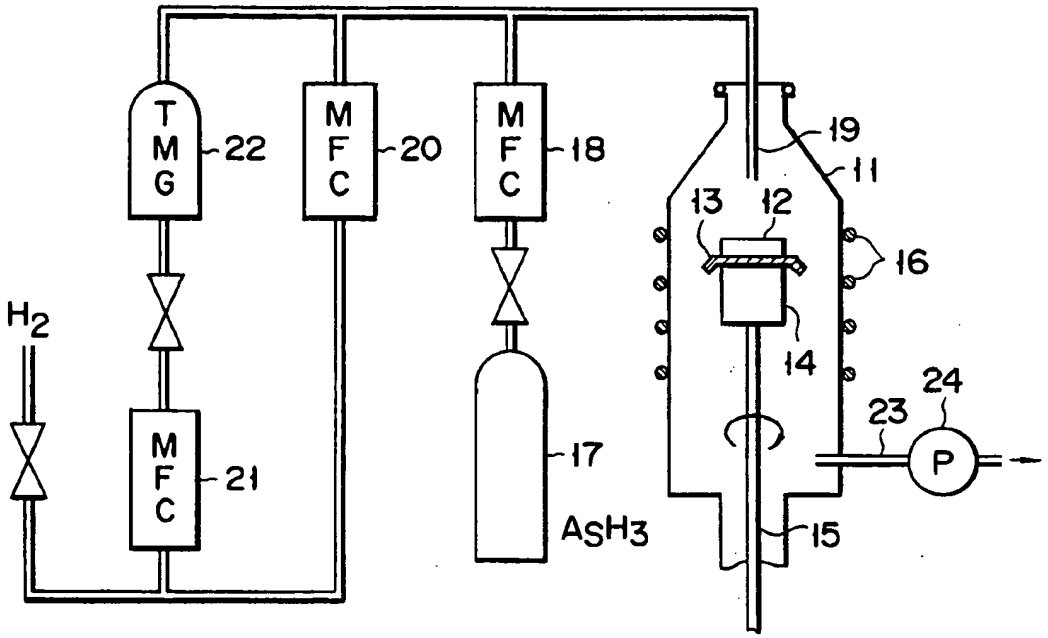

TMG
22
MFC
20
MFC
18
19
11
13
12
16
H2
14
24
23
MFC
21
17
P
AsH3
15

FIG. 1

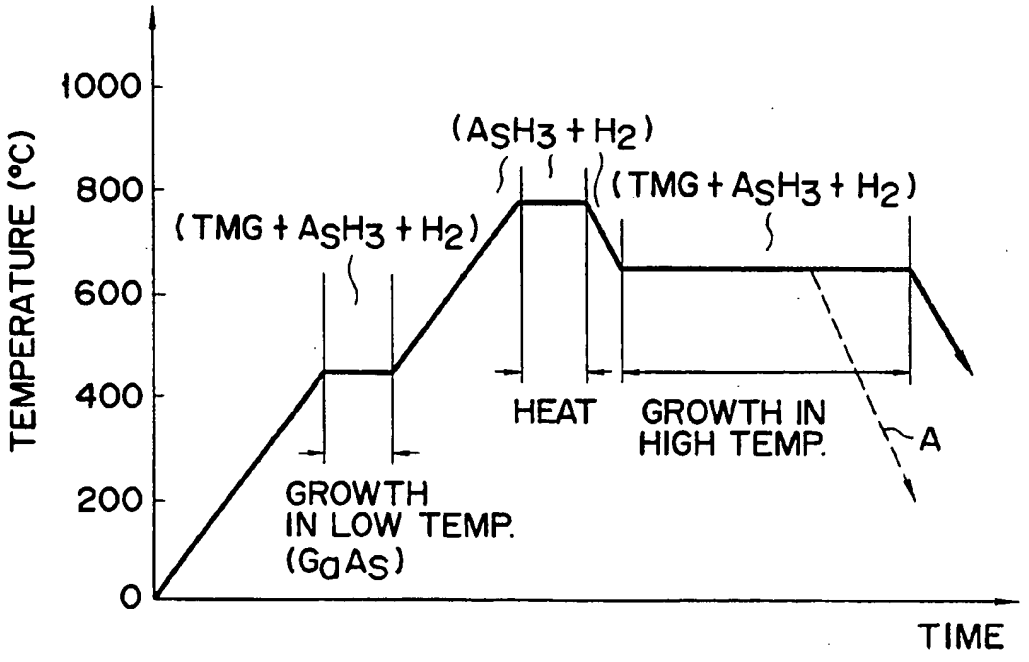

1000
800
600
400
200
0
TEMPERATURE (°C)
(AsH3 + H2)
(TMG + AsH3 + H2)
(TMG + AsH3 + H2)
HEAT
GROWTH IN
HIGH TEMP.
A
GROWTH
IN LOW TEMP.
(GaAs)
TIME

FIG. 2

FIG. 3A

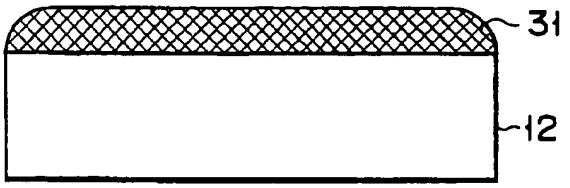


FIG. 3B

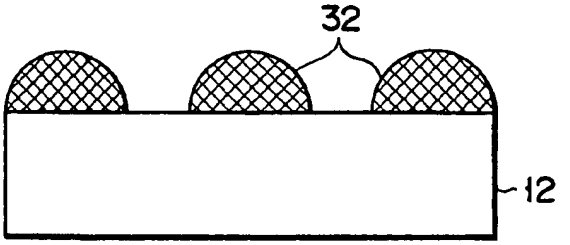


FIG. 3C

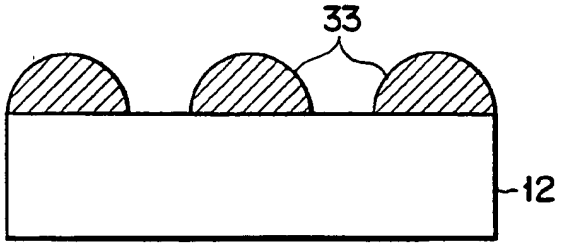


FIG. 3D

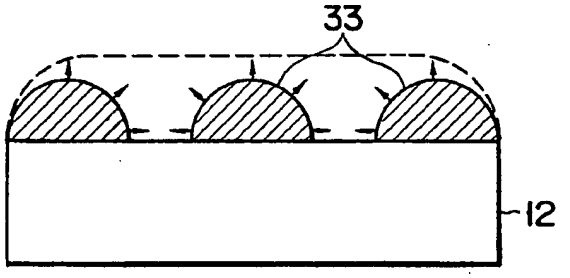
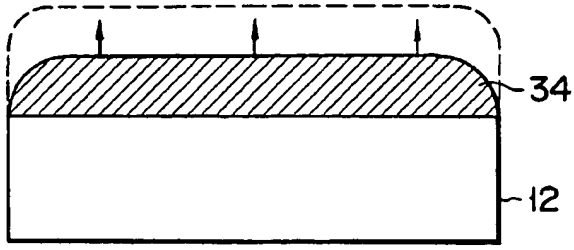


FIG. 3E



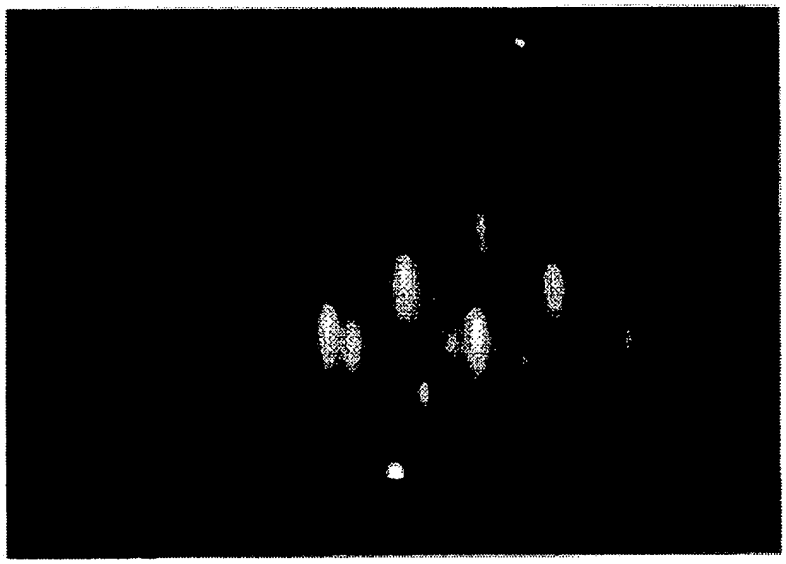


FIG. 4

FIG. 5

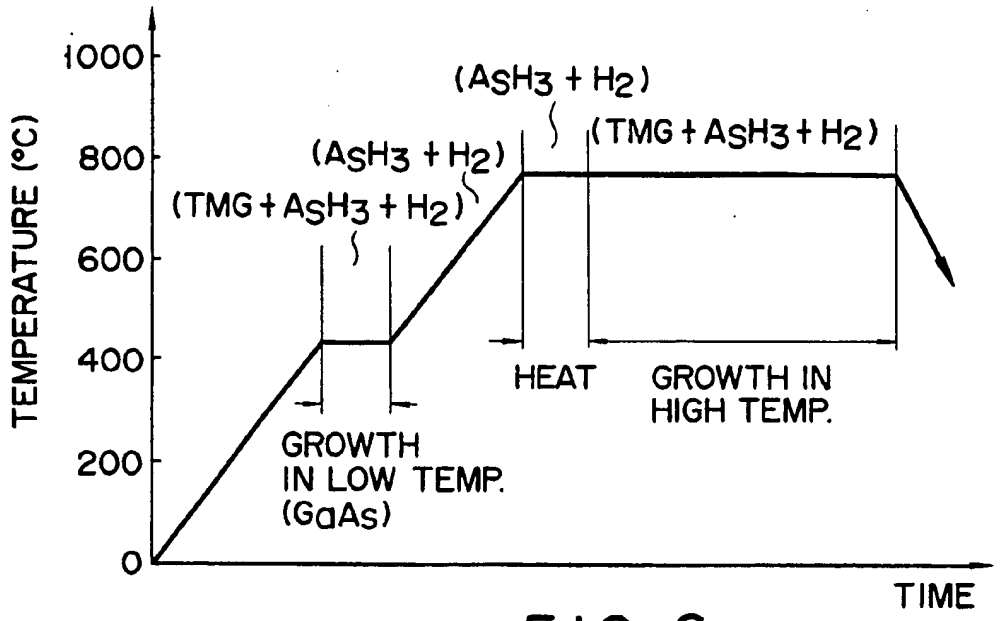


FIG. 6

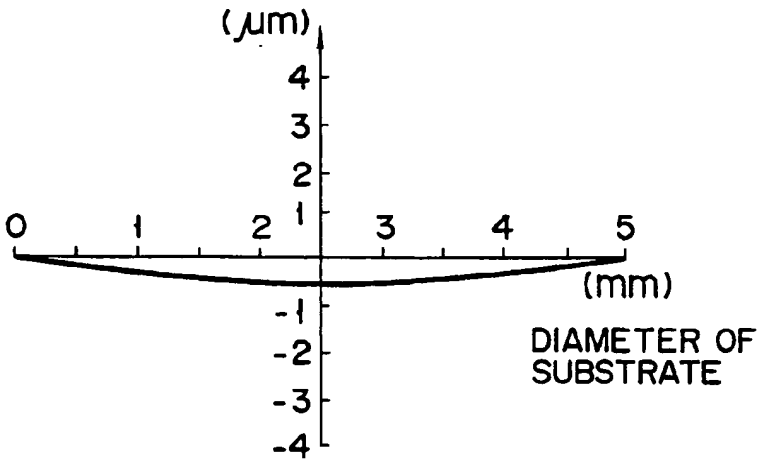


FIG. 7

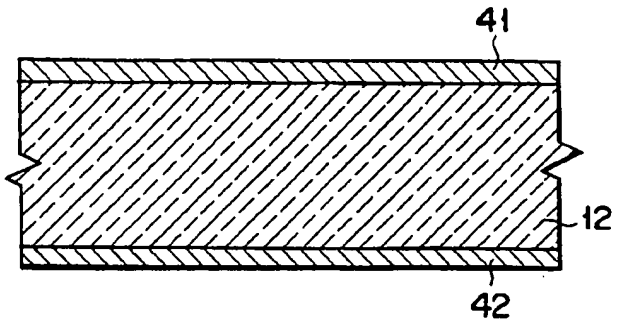


FIG. 8

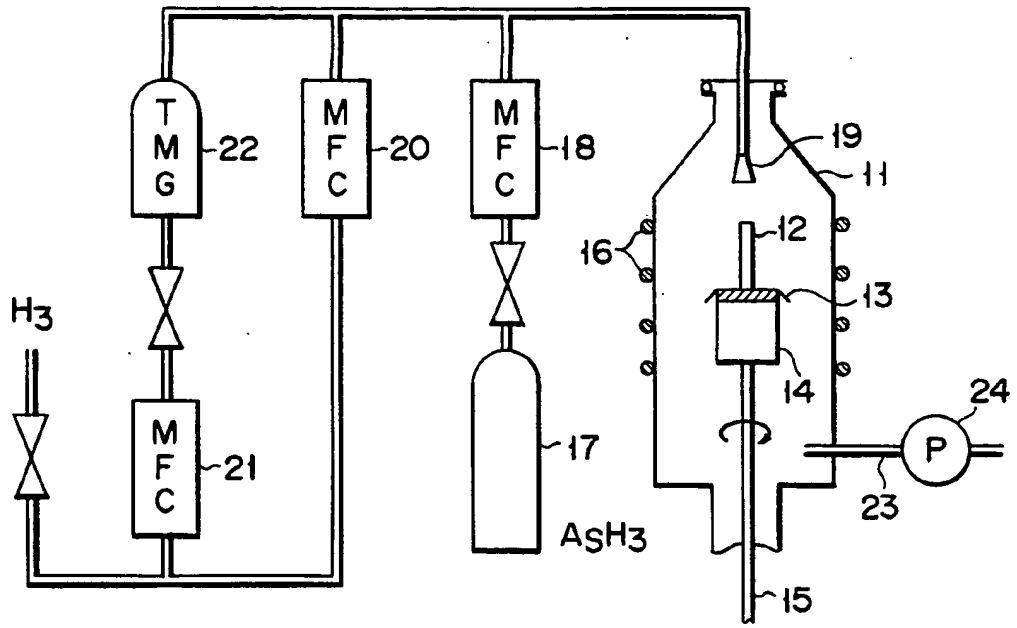

T
M
G
22
M
F
C
20
M
F
C
18
19
11
12
16
13
14
24
P
23
H3
M
F
C
21
17
AsH3
15

FIG. 9

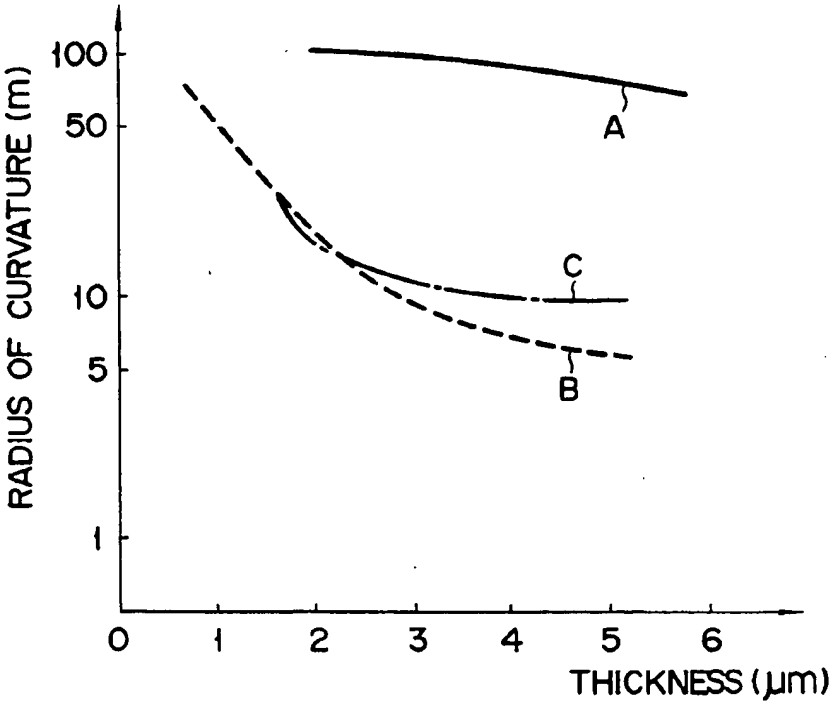

RADIUS OF CURVATURE (m)
100
50
10
5
1
A
C
B
0
1
2
3
4
5
6
THICKNESS (μm)

FIG. 10

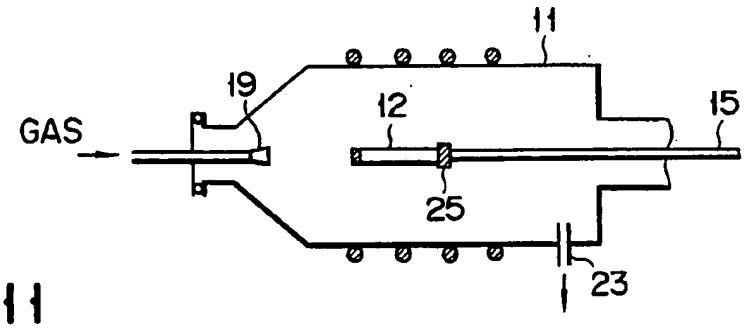


FIG. 11

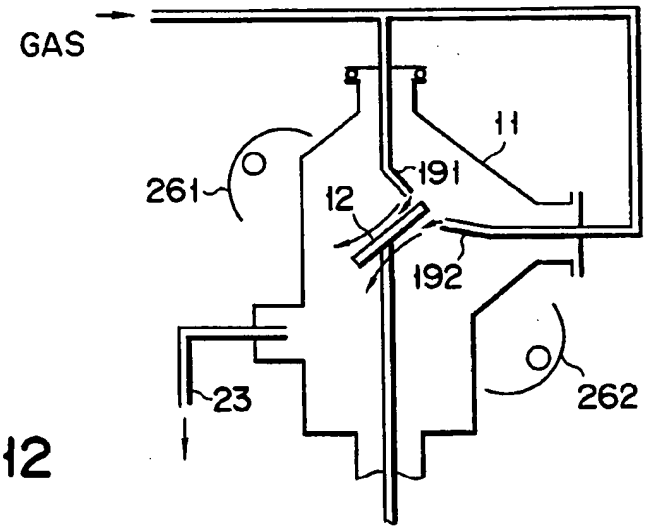


FIG. 12

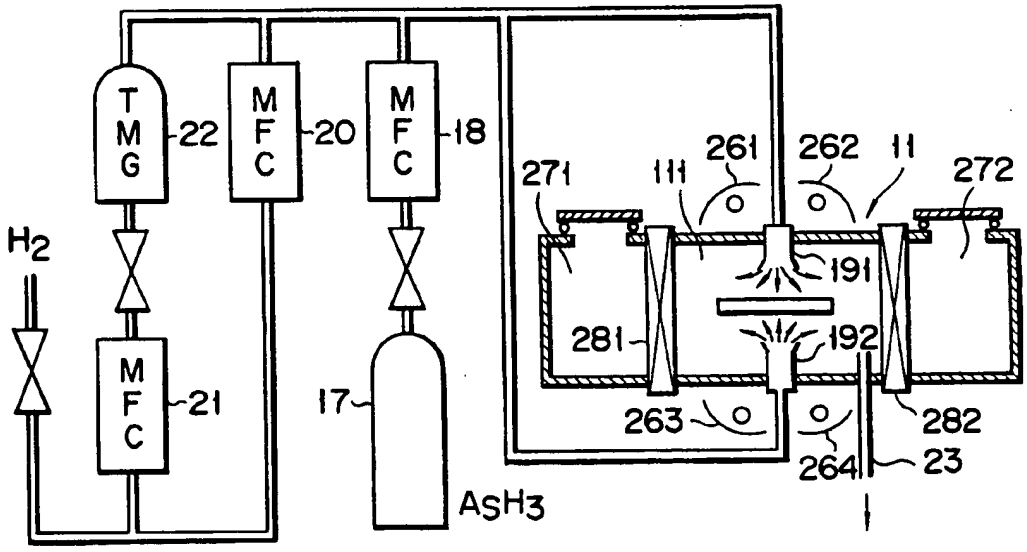


FIG. 13

SEMICONDUCTOR DEVICE WITH VAPORPHASE GROWN EPITAXIAL

This is a continuation of application Ser. No. 07/845,812, filed on Mar. 9, 1992, which was abandoned upon the filing hereof which was a continuation of application Ser. No. 07/420,721 filed Oct. 11, 1989, now abandoned, which was a continuation of application Ser. No. 07/123,549 filed Nov. 20, 1987, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor device with a vapor-phase grown epitaxial layer, and to a method of manufacturing the same, more particularly, to a method for causing vapor-phase epitaxial growth, on the surface of a semiconductor substrate of silicon or the like, of GaAs or a like substance having a different lattice constant from that of the substrate, and to a semiconductor device having the vapor-phase epitaxial layer.

It is well known in the art that when fabricating a semiconductor device, an epitaxial layer is formed on a semiconductor substrate by causing vapor-phase growth on the substrate surface of a semiconductor having a different lattice constant from that of the substrate.

For instance, a Group III and V element compound semiconductor, e.g., GaAs or InP, is epitaxially grown on a semiconductor substrate, such as a silicon substrate. When a semiconductor of GaAs, InP, or a like compound is epitaxially grown on the silicon substrate surface, there is a lattice mismatch factor with respect to the silicon constituting the substrate. This factor is 4.1% in the case of GaAs and 8.1% with InP. Therefore, if a GaAs layer is formed on a silicon substrate by growing GaAs thereon, the resultant epitaxial layer will have considerable defects and inferior surface shape.

With the aim of solving this problem, it has been proposed to form an intermediate layer as a super-lattice constitution element between the silicon substrate and GaAs layer, so as for this intermediate layer to absorb the lattice mismatch between silicon and GaAs, this method being disclosed in Japanese Patent Laid-Open Publication Sho 61 (1985) - 91,098.

However, where such an intermediate layer is formed, mixture crystal and very thin films must be controlled repeatedly in the epitaxial layer formation process, and complicated process control is required.

It is taught to cause growth of GaAs directly on a silicon substrate, and it is well known that a mirror surface can be obtained by means of a two-step growth process. In this case, however, a resultant hetero-epitaxial layer contains a large number of transitions and other defects.

For example, when a thin film of GaAs is formed on a silicon substrate, warping of the resultant wafer results when a high level of heat is applied thereto, due to silicon and GaAs having different coefficients of thermal expansion.

SUMMARY OF THE INVENTION

An object of the invention is to provide a method for causing epitaxial growth of a layer of GaAs or a like substance, on a semiconductor substrate of silicon or the like.

Another object of the invention is to provide a method of causing vapor-phase epitaxial growth, which permits an epitaxial layer having less transitions and of sufficient quality to be formed when GaAs is epitaxially grown on a semiconductor substrate by means of a two-step growth process.

Another object of the invention is to provide a semiconductor device the semiconductor substrate of which is free from warping or like deformation, even if it has an epitaxial growth layer composed of a substance having a different coefficient of thermal expansion from that of the semiconductor device, and a method of manufacturing the same semiconductor device.

More specifically, using the method of vapor-phase epitaxial growth according to the invention, a semiconductor substance having a different lattice constant from that of the substrate is formed by low temperature growth as amorphous crystal, polycrystal, or bicrystal on the semiconductor substrate, and subsequently the resultant thin film, having been grown, is rendered into an island-like single crystal. Then, high temperature growth of this island-like single crystal is caused to happen, whereby a growth layer of the semiconductor substance is formed on the semiconductor substrate surface.

In the above way, in a first step, a low temperature growth layer is formed as a GaAs thin film, for instance, by low temperature growth on the semiconductor substrate. This thin film is thermally treated to form an island-like single crystal, which is then subjected to high temperature heat treatment, whereby a high quality epitaxial growth layer having less transitions can be obtained.

Such epitaxial layers are formed on both sides of a semiconductor substrate. By so doing, the generation of warping or like deformation of the semiconductor substrate can be eliminated, as a result of which a highly reliable semiconductor integrated circuit or the like can be obtained, even when the semiconductor substances constituting the semiconductor substrate and epitaxial growth layer have different coefficients of thermal expansion.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic view showing an apparatus for carrying out an embodiment of the vapor-phase epitaxial growth method according to the invention;

FIG. **2** is a graph showing a temperature program used when causing epitaxial growth by means of the apparatus shown in FIG. **1**;

FIGS. **3**A to **3**E are views for explaining an epitaxial layer growth process when epitaxial growth is caused according to the temperature program;

FIGS. **4** and **5** are photographs of the crystal structure of a growth layer resulting from use of the epitaxial growth process noted above;

FIG. **6** is a graph showing a growth temperature program for explaining a second embodiment of the vapor-phase epitaxial growth method according to the invention;

FIG. **7** is a view showing warping when an epitaxial growth layer is formed on one surface of a semiconductor substrate;

FIG. **8** is an exaggerated sectional view showing a semiconductor device having vapor-phase epitaxial layers;

FIG. **9** is a schematic view showing an apparatus used for epitaxial growth when fabricating the semiconductor device as shown in FIG. **8**;

FIG. **10** is a graph for explaining the relation between the thickness of epitaxially grown GaAs thin film and the radius of curvature of warping of the semiconductor substrate; and

FIGS. 11 to 13 are views showing respective examples of apparatuses used forming an epitaxial growth layer on each principal surface of the semiconductor substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows an apparatus for forming an epitaxial growth layer on a semiconductor substrate. The apparatus comprises reaction vessel **11** made of quartz.

Semiconductor substrate **12**, of silicon for instance, on which an epitaxial growth layer is to be formed, is placed on quartz tray **13**, which is then disposed in reaction vessel **11**. Quartz tray **13** with semiconductor substrate **12** thereon, is transported from a load lock chamber (or a spare chamber) by an automatic or manual transport mechanism into reaction vessel **11**. Quartz tray **13** is supported on graphite susceptor **14**. Susceptor **14** is supported by work coil **15**. By work coil **15**, susceptor **14** is disposed together with semiconductor substrate **12** at a predetermined position in reaction vessel **11**.

High frequency induction coil **16** is disposed such that it surrounds reaction vessel **11**. High frequency power is supplied selectively to high frequency coil **16**. Semiconductor substrate **12** is induction heated with the high frequency power being supplied. Although not particularly shown in the Figure, work coil **15** is provided with a temperature sensor consisting of a thermocouple or the like. The temperature sensor detects the temperature of semiconductor substrate **12**. The high frequency power supplied to induction coil **16** is controlled according to a detection signal from the temperature sensor, and the operating temperature, i.e., growth temperature of semiconductor substrate **12**, is controlled with high accuracy.

Material gas (AsH_3) is supplied from material gas vessel **17** through mass flow controller **18** into reaction vessel **11**. Accurately flow-controlled material gas is supplied form nozzle **19** into reaction vessel **11**, so that it can be sprayed against the epitaxial growth surface of semiconductor substrate **12**.

H_2 gas is supplied as carrier gas through mass flow controller **20** into reaction vessel **11**. The H_2 carrier gas is supplied through mass flow controller **21** into trimethyl gallium (TMG) vessel **22**. A material gas, for example, trimethyl gallium is supplied to nozzle **19** to be injected into reaction vessel **11**.

Reaction vessel **11** is provided with discharge port **23**, in which oil pump **24** is provided to forcibly discharge gas from reaction vessel **11**. During the growth, the interior of reaction vessel **11** is held under atmospheric pressure. When causing reduced pressure growth, the gas in reaction vessel **11** is discharged through discharge port **23**, so that the interior of reaction vessel **11** is held under a predetermined reduced pressure.

To uniformalize the thickness of the growth layer formed on the surface of semiconductor substrate **12**, susceptor **14** is rotated by work coil **15**, so that semiconductor substrate **12** is rotated with its surface is coincident with the surface of susceptor **14**. In reaction vessel **11**, a GaAs film is formed on the surface of semiconductor substrate **12**. The growth of the GaAs film is carried out according to a temperature program shown in FIG. **2**.

In a process for causing the growth of an GaAs film on the surface of semiconductor substrate **12**, semiconductor substrate **12** consisting of silicon is placed on quartz tray **13**, which is then transported from a preparation chamber (not shown) to susceptor **14** in reaction vessel **11**. Semiconductor substrate **12** is disposed at a predetermined position in reaction vessel **11** by work coil **15**. In this state, high frequency power is selectively supplied to high frequency coil **16**, thus permitting selective temperature increase control of semiconductor substrate **12**.

The process of control in the interior of reaction vessel **11** will now be described with reference to a temperature program shown in FIG. **2**. The temperature of the interior of reaction vessel **11** is increased from room temperature to 450° C. with semiconductor substrate **12** disposed at a predetermined position in reaction vessel **11**. When the temperature is elevated to 450° C., it is held at this value, and in this state trimethyl gallium (TMG) and arsine (AsH_3) as material gas are introduced in predetermined quantities together with the carrier gas (H_2) from nozzle **19** into reaction vessel **11** such that these gases touch the surface of semiconductor substrate **12**. As shown in FIG. **3**A, thin film **31** of GaAs is low-temperature grown on the surface of semiconductor substrate **12**.

The thickness of GaAs thin film **31** formed on the surface of semiconductor substrate **12** is suitably about 100 angstroms, and GaAs is suitably amorphous, polycrystalline and bicrystalline. FIG. **4** shows a (RHEED) image of the GaAs layer obtained by the low-temperature growth.

When GaAs thin film **31** is formed in this way by the low-temperature growth, the supply of trimethyl gallium is stopped, and the temperature of semiconductor substrate **12** is elevated up to 750° C. in an atmosphere consisting of AsH_3 and H_2 gases. Then the temperature is stablized at 750° C., the system is subjected to a thermal treatment for about 5 minutes in the atmosphere noted above.

In the step of the temperature increase up to 750° C., GaAs thin film **31** formed by the low-temperature growth on the surface of semiconductor substrate **12**, is like island **32** consisting of coagulation of atoms as shown in FIG. **3**B, and island-like single crystal cores **33** as shown in FIG. **3**C are formed by a thermal treatment in a temperature state at 750° C. Through such thermal treatment, the lattice mismatch between semiconductor substrate **12** consisting of silicon and GaAs film grown on the surface of substrate **12** is alleviated.

FIG. **5** shows a RHEED image, in which island-like single crystal cores are formed on semiconductor substrate **11**. It will be seen that island-like single crystals can be clearly recognized.

After this thermal treatment, the temperature of semiconductor substrate **12** in reaction vessel **11**, i.e., growth temperature, is reduced to 650° C. In the state of the reduced temperature, trimethyl gallium is supplied together with AsH_3 and carrier gas H_2 into reaction vessel **11**.

Further, the GaAs layer formed on semiconductor substrate **12** is subjected to growth in the transversal direction as shown in FIG. **3**D, and then the GaAs layer is subjected to homoepitaxial growth up to a desired thickness as shown in FIG. **3**E.

Epitaxial growth layer **34** of GaAs formed in this way, is thought to have high efficiency of photoluminecsence, and it constitutes a GaAs heteroepitaxial growth device having high crystal property.

When the GaAs layer formed obtained by the low-temperature growth becomes as thick as approximately 1,000 angstroms so that island-like single crystals are formed by a thermal treatment at 750° C., an intent to cause growth of an GaAs film by supplying trimethyl gallium at 650° C. leads to the formation of a film having inferior

crystal property due to inferior surface homology of the growth layer.

When the high temperature growth process for causing growth of single crystals is omitted as shown by dashed line A in the temperature program shown in FIG. **2**, the GaAs growth layer formed on the surface of semiconductor substrate **12** has inferior surface homology, and the crystal property is inferior.

FIG. **6** shows a different example of the temperature program in a vapor-phase epitaxial growth process shown in FIG. **6**. In this example, the high temperature growth process for causing growth of single crystals is performed in an atmosphere at a temperature of 750° C. like a 750° C. thermal treatment process for forming island-like single crystal cores. More specifically, after island-like single crystal cores have been formed through a thermal treatment at a high temperature of 750° C. in an atmosphere "AsH_3+H_2", at the same temperature trimethyl gallium is introduced into reaction vessel **11** for causing high temperature growth of the GaAs layer.

The embodiments so far have concerned with the case of causing epitaxial growth of the GaAs layer on a silicon substrate. However, even in case when the GaAs layer is grown on SOS (silicon on sapphire), a crystal grown layer is obtained by a similar epitaxial growth method. Further, the semiconductor substance to be grown, is not limited to GaAs, but similar growth methods can be carried out even in case when such semiconductor substance as AlGaAs, InP and SiC is formed on a semiconductor substrate having a different lattice constant from that of such semiconductor substance.

The technique of causing epitaxial growth of GaAs on a silicon substrate formed on the embodiment, is effective for the formation of ICs utilizing GaAs having large areas and substrates for solar batteries, and it has high usefulness for the realization of GaAs/Si compound integrated circuit in which a GaAs device is formed on a silicon IC.

Assuming a case when a GaAs thin film is formed on the surface of a silicon substrate, while the coefficient of thermal expansion of GaAs is 2.6×10^{-6}°C.$^{-1}$ the coefficient of thermal expansion of silicon is 5.9×10^{-6}°C.$^{-1}$. Thus, when a GaAs thin film is formed by crystal growth directly on the silicon substrate, a strong tensile force is produced in the GaAs thin film according to temperature changes, and a force for generating the warping as shown in FIG. **7** acts on the silicon substrate. Where the thickness of the GaAs thin film exceeds 3 to 4 μm, a problem of generation of cracks is posed.

FIG. **7** shows the results of measurement of the warping of the silicon substrate on a sample, with a silicon substrate diameter of 5 mm, a substrate thickness of 500 μm and a GaAs thin film thickness of 4.6 μm, using a probe-type step gauge.

FIG. **8** is a sectional view showing a semiconductor device constructed by taking the foregoing into considerations. Semiconductor substrate **12** consisting of silicon has a thickness of 500 μm. GaAs thin films **41** and **42** are formed on the two principal surfaces of substrate **12**. GaAs thin films **41** and **42** have substantially a uniform thickness. For example, the thickness is set to 4.6 μm.

Such GaAs thin films **41** and **42** are formed by vapor-phase epitaxial growth using the apparatus as shown in FIG. **9**.

The apparatus shown in FIG. **9** is basically the same as the apparatus shown in FIG. **1**, and like parts are designated by like reference numerals. With this apparatus, semiconductor substrate **12** is erected on quartz tray **13** in reaction vessel **11** such that its opposite surfaces are exposed. Nozzle **19** is disposed above semiconductor device **12**, such that reaction gas issued from nozzle **19** effectively touches the opposite surfaces of semiconductor substrate **12**.

By setting semiconductor substrate **12** in reaction vessel **11** and effecting epitaxial growth treatment according to the temperature program as shown in FIGS. **2** or **6**, thin films **41** and **42** consisting of a semiconductor substrate are formed to an equal thickness on the opposite surfaces of semiconductor substrate **12**.

FIG. **10** shows the results of measurement of the warping of substrate conducted by the inventor. The abscissa is taken for the thickness of the GaAs thin film, and the ordinate is taken for the logarithmic scale of the radius of curvature of the substrate. In the Figure, solid curve A shows an example of growth of GaAs thin films **41** and **42** formed on the opposite surfaces of semiconductor substrate **12** as shown in FIG. **8**. The dashed curve B shows an example of growth of the GaAs thin film formed on one surface of the semiconductor substrate. The phantom line curve C shows an example of the growth of a GaAs thin film on approximately 2,000 angstrom intermediate layers of of GaP/GaAsP and GaAsP/GaAs formed on the semiconductor substrate.

The thickness of the ordinary GaAs thin film is 3 to 5 μm. As is apparent from the results of measurement, with the semiconductor device as shown in FIG. **8** having the characteristic A, the radius of curvature of is greater by approximately one only of magnitude than that of the prior art structures having the characteristics B and C.

More specifically, with the semiconductor device shown in FIG. **8**, ICs are formed on GaAs thin film **41** formed on one principal surface of semiconductor substrate **12**, and GaAs thin film **42** on the other principal surface is formed to reduce the generation of warping of substrate **12**. However, thin film **42** has a thickness of approximately 1/100 of the thickness of semiconductor substrate **12**, and the thermal conductivity of substrate **12** is not influenced by thin film **42**. Further, it is of course possible to form ICs on GaAs thin film **42** on the other principal surface.

To form vapor-phase epitaxial growth layers on the opposite sides of the semiconductor substrate, reaction vessel **11** may be modified as shown in FIG. **9**. Also, it is possible to construct reaction vessel **11** to be horizontal as shown in FIG. **11**. In this case, semiconductor substrate **12** is held by holder **25** or the like mounted on work coil **15** such that the reaction gas issued form nozzle **19** touches the opposite surfaces of semiconductor substrate **12**.

FIG. **12** shows a further example of reaction vessel **11**. Semiconductor substrate **12** is set in reaction vessel **11** in an inclined state, and two nozzles **191** and **192** are set such that reaction gas is supplied to the opposite side surfaces of semiconductor substrate **12**. The same gas is supplied from nozzles **191** and **192** to flow along the opposite surfaces of semiconductor substrate **12**.

In order to prevent vortex flow of material gas supplied from nozzles **191** and **192**, it is necessary to consider the amount of gas supplied, and the shape and positional relation of nozzles **191** and **192** and reaction vessel **11**.

In the embodiment so far, high frequency induction coils are used for heating semiconductor substrate **12** in reaction vessel **11**, and high frequency power supplied to the induction coils is controlled so that semiconductor substrate **12** is heated selectively and in a temperature controlled state.

However, semiconductor substrate **12** may be heated by various other means as well. For example, it is possible to

use infrared lamps **261** and **262** as shown in FIG. **12**. In this case, it is possible to use stainless steel (SUS) instead of quartz as the material of reaction vessel **11**.

FIG. **13** shows a further example of reaction vessel. Reaction vessel **11** has reaction chamber **111** and first and second spare rooms **271** and **272** provided on the opposite sides. Reaction chamber **111** is defined with respect to first and second spare chambers **271** and **272** by gate valves **281** and **282**. Semiconductor substrate **12** is transported by a transport mechanism utilizing a belt mechanism or H_2 gas. When gate valve **281** is open, substrate **12** is transported from first spare chamber **271** into reaction chamber **111**. When gate valve **282** is open, it is transported from reaction chamber **111** to second spare chamber **272**. Two nozzles **191** and **192** are provided in reaction chamber **111** such that they face each other. Semiconductor substrate **12** is transported to a position between nozzles **191** and **192**. In its position between nozzles **191** and **192**, substrate **12** is heated by infrared lamps **261** to **264**.

In this apparatus, semiconductor substrate **12** is set in first spare chamber **271**. Spare chamber **271** is evacuated to a vacuum degree of approximately 10 Torr by a turbomolecular pump and oil rotation pump (these pumps being not shown). Subsequently, H_2 gas is introduced into first spare chamber **271** to produce the same pressure condition as in reaction chamber **111**. In this state, gate valve **281** is opened, and semiconductor substrate **12** is transported into reaction chamber **111**.

In reaction chamber **111**, it is located at a position between nozzles **191** and **192** as shown, and in this state material gas is supplied from nozzles **191** and **192**. Then, semiconductor substrate **12** is temperature controlled and the contents of material gas are selected, whereby GaAs thin films are grown on the opposite sides of semiconductor substrate **12**. When predetermined GaAs thin films have been grown on the opposite side surfaces of semiconductor substrate **12**, gate valve **282** is opened, and semiconductor substrate **12** is transported into second spare room **272** to be taken out.

What is claimed is:

1. A method of manufacturing a semiconductor device having an epitaxial layer formed on a surface of a semiconductor substrate, said method comprising the steps of:

placing said substrate in a reaction chamber provided with heating means so as to permit selective setting of temperature of said semiconductor substrate;

forming a low-temperature growth layer, as a thin film having a thickness, on the surface of said semiconductor substrate, said thin film being formed of a semiconductor substance having a different lattice constant from that of said semiconductor substrate, said forming step including the steps of:

supplying a material gas which is a mixture of gases containing an organometallic gas as a material of said semiconductor substance into said reaction chamber, and

forming the semiconductor substance to a thickness less than 200 angstroms;

thermally treating the low-temperature growth layer at a temperature higher than that in said forming step, said temperature being sufficient for forming a plurality of island-like monocrystal cores from said thin film, said thermally treating step including the steps of:

stopping the supply of said organometallic gas,

elevating the temperature of said semiconductor substrate to about 750° C. to cause coagulation of the atoms of the semiconductor material constituting the low temperature growth layer formed in said forming step, and

maintaining the temperature of said semiconductor substrate at about 750° C. while the flow of said organometallic gas is stopped to reduce lattice mismatch between the island-like monocrystaline cores and the semiconductor substrate surface; and

causing high-temperature growth of said semiconductor substance on said semiconductor substrate having said island-like monocrystal cores, said causing step including the step of supplying a material gas containing said organometallic gas as the material of said semiconductor substance into said reaction chamber while said semiconductor substrate is held at a high temperature, thereby generating epitaxial growth of said island-like monocrystal cores.

2. A method according to claim **1**, wherein said semiconductor substrate consists of silicon, and said semiconductor substance is a Group III and V element compound semiconductor.

3. A method according to claim **2**, wherein said Group III and V element compound semiconductor is GaAs.

4. A method according to claim **2**, wherein said Group III and V element compound semiconductor is InP.

5. A method according to claim **1**, wherein the material gas containing said semiconductor substance contains trimethyl gallium and arsine.

6. A method according to claim **1**, further comprising the steps of:

setting said semiconductor substrate in said reaction chamber such that two principal surfaces of said semiconductor substrate are exposed;

forming a plurality of island-like monocrystal cores on the two principal surfaces during said thermally treating step; and

simultaneously forming first and second thin films respectively on the two principal surfaces by epitaxially growing said monocrystal cores on each of said two principal surfaces during said causing step.

7. A method according to claim **6**, wherein said causing step includes forming first and second semiconductor thin films having an equal thickness.

8. A method according to claim **1**, wherein said placing step includes growing the thin film is in an amorphous or polycrystalline state at a low temperature.

9. A method for forming a GaAs layer on a silicon substrate, said method comprising the steps of:

placing a silicon substrate within a reaction chamber;

heating the silicon substrate to about 450° C.;

supplying a carrier gas, arsine and trimethyl gallium gas into the reaction chamber;

maintaining the silicon substrate at about 450° C. for a time, while continuously supplying the carrier gas, arsine and trimethyl gallium gas into the reaction chamber thereby forming a thin GaAs layer having a thickness at low temperature on the silicon substrate;

stopping the supply of trimethyl gallium gas into the reaction chamber;

raising the temperature of the silicon substrate to about 750° C. while continuously supplying only the carrier gas and arsine into the reaction chamber, thereby enabling the thin GaAs layer having the thickness on the silicon substrate to be transformed into island-shaped monocrystals;

maintaining the temperature of the silicon substrate at about 750° C. for a predetermined time to reduce a

lattice mismatch between the island-shaped monocrystals and the silicon substrate; and

supplying the carrier gas, arsine and trimethyl gallium gas into the reaction chamber;

lowering the temperature of the silicon substrate to about 650° C.; and

maintaining the silicon substrate at about 650° C. for a time, while continuously supplying the carrier gas, arsine and trimethyl gallium gas into the reaction chamber, thereby growing the island-shaped GaAs monocrystals at high temperature on the silicon substrate, into a thick GaAs layer.

10. A method for forming a GaAs layer on a silicon substrate, said method comprising the steps of:

placing a silicon substrate within a reaction chamber;

heating the silicon substrate to about 450° C.;

supplying a carrier gas, arsine and trimethyl gallium gas into the reaction chamber;

maintaining the silicon substrate at about 450° C. for a time, while continuously supplying the carrier gas, arsine and trimethyl gallium gas into the reaction chamber thereby forming a thin GaAs layer having a thickness at low temperature on the silicon substrate;

stopping the supply of trimethyl gallium gas into the reaction chamber;

raising the temperature of the silicon substrate to about 750° C. while continuously supplying only the carrier gas and arsine into the reaction chamber, thereby enabling the thin GaAs layer having the thickness on the silicon substrate to be transformed into island-shaped monocrystals;

maintaining the temperature of the silicon substrate at about 750° C. for a predetermined time to reduce a lattice mismatch between the island-shaped monocrystals and the silicon substrate; and

supplying the carrier gas, arsine and trimethyl gallium gas into the reaction chamber; and

maintaining the silicon substrate at about 750° C. for a predetermined time, while continuously supplying the carrier gas, arsine and trimethyl gallium gas into the reaction chamber, thereby growing the island-shaped GaAs monocrystals at high temperature on the silicon substrate, into a thick GaAs layer.

11. A method according to claim **1**, wherein said thin film formed on the surface of said semiconductor substrate has a thickness of approximately 100 angstroms.

12. A method of manufacturing a semiconductor device having an epitaxial layer formed on a surface of a semiconductor substrate, said method comprising the steps of:

placing said substrate in a reaction chamber provided with heating means so as to permit selective setting of temperature of said semiconductor substrate;

forming a low-temperature growth layer, as a thin film having a uniform thickness, on the surface of said semiconductor substrate, said thin film being formed of a semiconductor substance having a different lattice constant from that of said semiconductor substrate, said forming step including the step of supplying a material gas which is a mixture of gases containing an organometallic gas as a material of said semiconductor substance into said reaction chamber;

thermally treating the low-temperature growth layer at a temperature higher than that in said low-temperature growth layer forming step, thereby enabling said thin film having the uniform thickness to transform into a plurality of island-like monocrystal cores, said thermally treating step including the steps of:

stopping the supply of said organometallic gas of said semiconductor substance,

elevating the temperature of said gases and of said semiconductor substrate to cause coagulation of the atoms of the semiconductor material constituting the low-temperature growth layer formed in said low-temperature growth forming step, and

extending the thermally treating step to reduce a lattice mismatch between the island-like monocrystal cores and the semiconductor substrate surface; and

causing high-temperature growth of said semiconductor substance on said semiconductor substrate having said island-like monocrystal cores, said causing step including the step of supplying a material gas containing said semiconductor substance into said reaction chamber while holding said semiconductor substance at a temperature lower than that of said thermally treating step, thereby generating epitaxial growth of said island-like monocrystal cores.

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